82358DT
EISA BUS CONTROLLER

- **Supports 82350 and 82350DT Chip Set Based Systems**
  - **— Mode Selectable for Either 82350 or 82350DT Based Systems**
  - **— Mode Defaults to 82350 Based Systems**
- **Socket Compatible with the 82358 (EISA Bus Controller)**
- **Provides EISA/ISA Bus Cycle Compatibility**
  - **— EISA/ISA Standard Memory or I/O Cycles**
  - **— EISA/ISA Wait State Cycles**
  - **— ISA No Wait State Cycles**
  - **— EISA Burst Cycles**
- **Supports Intel386™ & Intel486™ Microprocessors**
- **Translates Host (CPU) and 82359 (DRAM Controller) Cycles to EISA/ISA Bus Cycles**
- **Generates ISA Signals for EISA Masters**
- **Generates EISA Signals for ISA Masters**
- **Supports 8-, 16-, or 32-bit DMA Cycles**
  - **— Type A, B, or C (Burst) Cycles**
  - **— Compatible Cycles**
- **Supports Host and EISA/ISA Refresh Cycles**
- **Generates Control Signals for Address and Data Buffers**
  - **— 82353 (ADP) and 82352 (EBB)**
- **Supports Byte Assembly/Disassembly for 8-, 16-, or 32-Bit Transfers**
- **Selectable Host (CPU) Posted Memory Write Support to EISA/ISA Bus**
- **Cache Controller (82385, 82395) Interface to Maximize Performance for 386 Based Systems**
- **Supports I/O Recovery Mechanism**
- **Generates CPU, 82385, and System Software Resets**
- **132-Pin PQFP Package**
- **Low Power CHMOS Technology**

(See Packaging Specification Order #240800, Package Type NG)

The 82358DT EISA Bus Controller is part of Intel's 82350 and 82350DT chip sets. There are five mode or function select pins which allow the 82358DT to be programmed for use in either 82350 or 82350DT based systems. The mode pins also provide support for posted memory write cycles to the EISA/ISA bus and Intel486™ burst support. The 82358DT defaults to 82350 mode and is 100% socket compatible with the 82358 (EBC).

The 82358DT interfaces the 386 and Intel486 microprocessors to the Extended Industry Standard Architecture (EISA) bus. It is used to facilitate bus cycles between the Host (CPU) bus and the EISA/ISA bus. In an 82350 system, the 82358DT interfaces to the cycle address and control signals of the Host bus. In an 82350DT system, the 82358DT interfaces to the cycle address and control signals of the 82359 DRAM controller. The 82358DT generates the appropriate data conversion and alignment control signals to implement an external byte assembly/disassembly mechanism for transferring data of different widths between the Host, EISA, and Industry Standard Architecture (ISA) buses. It also provides the cycle translation between the Host, EISA, and ISA buses.

The 82358DT is tightly coupled with the 82357 DMA controller (ISP) to run 8-. 16-, or 32-Bit EISA/ISA DMA transfers.

The 82358DT features hardware enforced I/O recovery logic to provide I/O recovery time between back- to-back I/O cycles.

The 82358DT provides special cache hardware interface signals to implement a high performance 386 based system with an 82385 or 82395 cache controller.

The 82358DT also provides resets to the Intel486, 80386, 82385, and other devices in the system to provide an integrated synchronous system reset.

March 1994

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82358DT EISA Bus Controller

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TABLES

1.0 82358DT TERMINOLOGY

82350 - The 82350 system environment (refer to Figure 2-1).

82350DT/ENHANCED - The 82350DT system environment selected for an enhanced configuration (refer to Figure 2-2 and section 4.1).

82350DT/BUFFERED - The 82350DT system environment selected for a buffered configuration (refer to Figure 2-3 and section 4.1).

HOST BUS - The bus that system memory and the Host CPU reside on. In an 82350DT system configured for buffered mode, this also includes the buffered bus.

EISA BUS - Extended **ISA** bus, a superset of the ISA bus. It includes all ISA bus features, along with extension to enhance performance and capabilities.

ISA BUS - The bus used in Industry Standard Architecture compatible computers. In the context of an EISA system, it refers to ISA subset of the EISA bus.

BUFFERED BUS - An additional bus that is provided in 82350DT buffered system environments for supplemental motherboard I/O devices (refer to Figure 2-3). This bus is transparent to the 82358DT. Peripheral devices on this bus are treated as host devices. In the context of this document, the host bus and buffered bus are referred to as one in the same: the host bus.

HOST CPU - The main system processor, located on the Host Bus. The HOST CPU uses the 82358DT and other system board facilities to interface to the EISA bus.

HOST MASTER - A 32-bit bus master located on the host bus (this includes the HOST CPU). In an 82350DT system configured for buffered mode, this also includes a 32-bit bus master located on the buffered bus. The 82358DT will convert the HOST control signals to EISA or ISA signals, when necessary.

EISA MASTER - A 16- or 32-bit bus master that uses the EISA signal set to generate memory or I/O cycles. The 82358DT will convert the EISA control signals to ISA signals, when necessary.

ISA MASTER - A 16-bit bus master that uses the ISA subset of the EISA bus for generation of memory or I/O cycles. This device must understand 8-bit or 16-bit ISA slaves, and route data to the appropriate byte lanes. It is not required to handle any of the signals associated with the extended portion of the EISA bus. The 82358DT will convert the ISA control signals to EISA signals, when necessary.

BUFFERED MASTER - A 32-bit bus master located on the buffered bus. A master on the buffered bus is perceived by the 82358DT as being a host master. In the context of this document, a reference to a host master also includes a buffered master.

HOST SLAVE - A 32-bit bus slave located on the host bus. In an 82350DT system configured for buffered mode, this also includes a 32-bit slave located on the buffered bus. It is the responsibility of the host slave to translate and understand EISA cycles.

EISA SLAVE - An 8-, 16-, or 32-bit memory/IO slave device that uses the extended signal set of the EISA bus to accept cycles from various masters. An EISA slave returns information about its type and data width using extended and ISA signals.

ISA SLAVE - An 8 or 16-bit slave that uses the ISA subset of the EISA bus to accept cycles from various masters. It returns ISA signals to indicate its type and data width.

BUFFERED SLAVE - A 32-bit bus slave located on the buffered bus. A slave on the buffered bus is perceived by the 82358DT as being a host slave. In the context of this document, a reference to a host slave also includes a buffered slave.

DMA DEVICE - A DMA device requests service by driving DREQx active. During a DMA transfer, the data is transferred between a memory slave and an I/O slave. The I/O slave is referred to as the DMA device.

MISMATCHED DATA SIZE - A master and slave that do not have equal data bus sizes (e.g. Host CPU accessing an 8-bit ISA slave, or a 16-bit DMA device accessing a 32-bit EISA memory slave).

ASSEMBLY/DISASSEMBLY - This occurs when the master/slave data bus sizes are mismatched. The 82358DT runs multiple cycles to route bytes to the appropriate byte lanes (byte swapping). For example, if a 32-bit host master is accessing an EISA or ISA 8-bit slave, the 82358DT will run four cycles to the 8-bit slave and route the bytes to appropriate byte lanes. For additional information, refer to section 4.4.

RE-DRIVE - This occurs when both the master and slave are on the EISA/ISA bus, and the master/slave data size combination is mismatched (e.g., 32-bit EISA master accessing an 8-bit ISA slave). During a re-drive cycle, the data is latched from the EISA/ISA bus, and then driven back onto the appropriate EISA/ISA byte lane. For additional information, refer to section 4.4.

DATA SIZE TRANSLATION - This is performed by the 82358DT when the master and slave data bus sizes do not match (e.g. 32-bit master/8-bit slave). During a data size translation, the 82358DT will perform one or more of the following operations, depending on the master/slave data size combination, master/slave type (Host/EISA/ISA), transfer direction (read/write), and the number of byte enables active: *data assembly, data copying (up or down), or data re-drive*. For additional information, refer to section 4.4.

CYCLE TRANSLATION - This is performed by the 82358DT when the master and slave are on different buses (Host/EISA/ISA). The 82358DT will translate the master protocol to the slave protocol, except in the case of an EISA or ISA master accessing a host slave. In this case, it is the responsibility of the host slave to translate and understand EISA cycles. For additional information, refer to section 4.3.

SYSTEM MEMORY - All memory in the system.

ISACMD - The ISA command signals (IORC#, IOWC#, MRDC#, MWTC#).

BACK-TO-BACK CYCLE - A back-to-back cycle is defined as a cycle on the EISA Bus where there is no idle time between the last CMD# signal and the next START# signal. This does not include the cycles within the boundries of an assemble or disassembly cycle.

2.0 INTRODUCTION

All descriptions in this document apply to both the 386 and i486 CPU, and the 82350 and 82350DT systems, unless otherwise stated.

2.1 82358DT System Architecture Overview

The 82358DT EISA Bus Controller is mode selectable to operate in either an 82350 or an 82350DT system environment (refer to Figures 2-1 through 2-3). In an 82350DT environment, the 82358DT is further mode selectable to operate in either an enhanced or buffered configuration. A detailed discussion on the various 82358DT modes and configurations can be found in section 4.1.

The 82358DT is located between the host (CPU) bus and the EISA/ISA bus, and provides the control signal translations necessary for bus to bus transfers. Cycles initiated on either bus are tracked by the 82358DT. The 82358DT translates EISA to ISA, ISA to EISA, and Host to EISA or ISA cycles. The 82358DT also breaks down bus cycles so that transfers between buses of different sizes or misaligned addresses function correctly. The data byte swap logic and address buffer control signals are generated directly from the 82358DT. These signals are used to control the 82353 Advanced Data Path (ADP) and the EISA Bus Buffer (EBB) devices.

In an 82350 based system, the 82358DT tracks and interfaces directly to the host bus. In an 82350DT based system, the 82358DT tracks host initiated cycles through the 82359 DRAM controller. When a host bus master initiates a cycle, and no host slave responds, the 82358DT forwards the cycle to the EISA/ISA bus. If back-to-back ISA I/O cycles are forwarded to the ISA bus, the 82358DT will insert delays between the back-to-back cycles for the purpose of I/O recovery. If a memory write cycle is forwarded to either an EISA or ISA slave, the 82358DT has the support capability to post the cycle.

The 82358DT provides the bridge between ISA and EISA devices on the EISA/ISA bus. The 82358DT translates cycles from EISA masters into cycles that ISA slaves can understand. Similarly, it translates cycles initiated by ISA masters into cycles that EISA slaves can understand. The 82358DT also performs byte assembly/disassembly for data transfers between devices on the EISA/ISA bus of varying data widths.

The 82357 Integrated System Peripheral (ISP), which contains the high performance EISA-compatible DMA controller, EISA arbitration, interrupt controller, refresh logic, and other integrated peripheral functions, interfaces to the 82358DT. When requested by the ISP, the 82358DT runs EISA or ISA bus cycles for DMA transfers and memory refreshes.

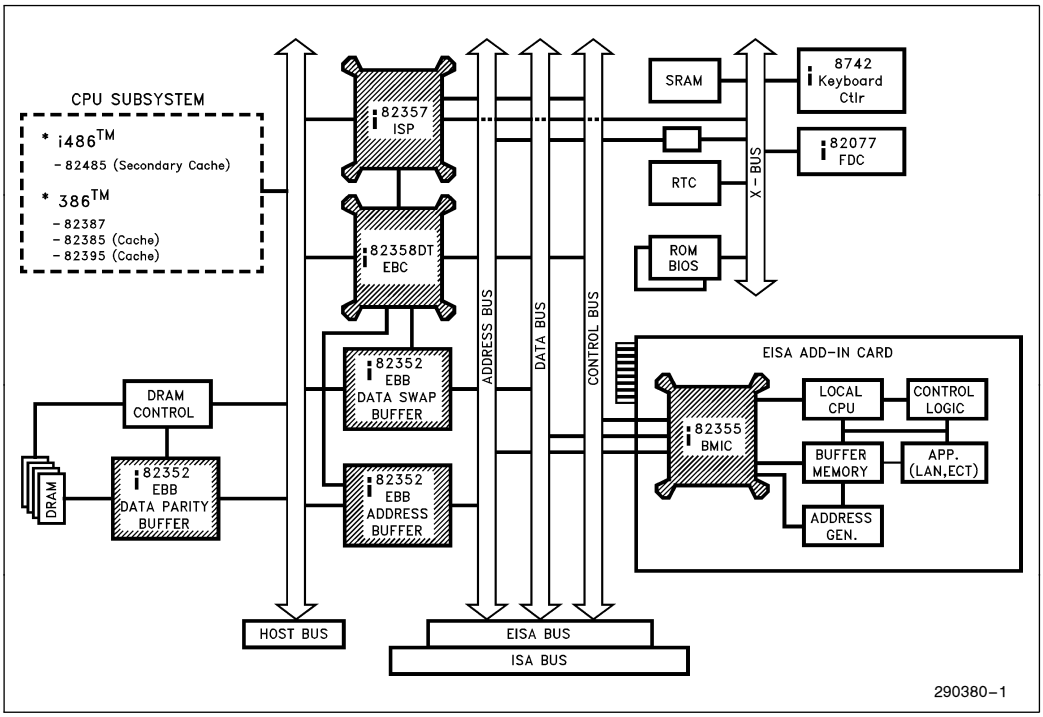


Figure 2-1. 82350 System Environment

The **82350 system** architecture is based on Intel's 82350 chip set. This chip set includes the 82358DT EISA bus controller, 82357 Integrated System Peripheral (ISP), and the 82352 EISA bus buffers (EBB).

The 82358DT provides the data and cycle translation between the host, EISA, and ISA buses during host, EISA, ISA, and DMA master cycles. The ISP provides the DMA function, refresh, system arbitration, interrupt control, timer/counter functions, and NMI control. The EBB provides the data swap logic and address path between the host, EISA, and ISA buses, and the data parity during memory accesses.

Also part of the EISA solution, is the 82355 Bus Master Interface controller (BMIC). The BMIC provides the EISA bus master functions necessary to interface a bus master add-in board to the EISA bus.

The 82350 system supports both 386 and i486 architectures.

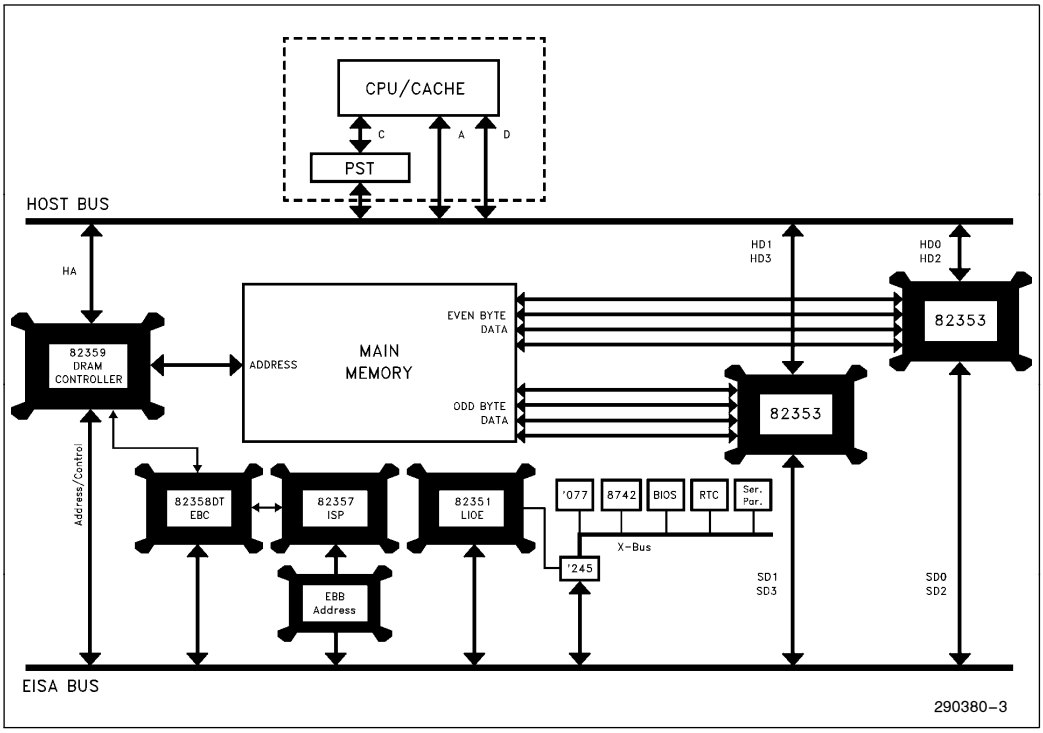


Figure 2-2. 82350DT System Environment (Enhanced Configuration)

The **82350DT/enhanced system** architecture is a superset of Intel's 82350 chip set. The 82350DT chip set builds upon the 82350 chip set by adding the following integrated functions: dual ported memory control, serial port support, bi-directional parallel port support, and real time clock support. To provide this additional support, the 82359 DRAM controller, 82353 Advanced Data Path (ADP), and the 82351 local I/O (LIOE) have been added to provide the 82350DT chip set functions.

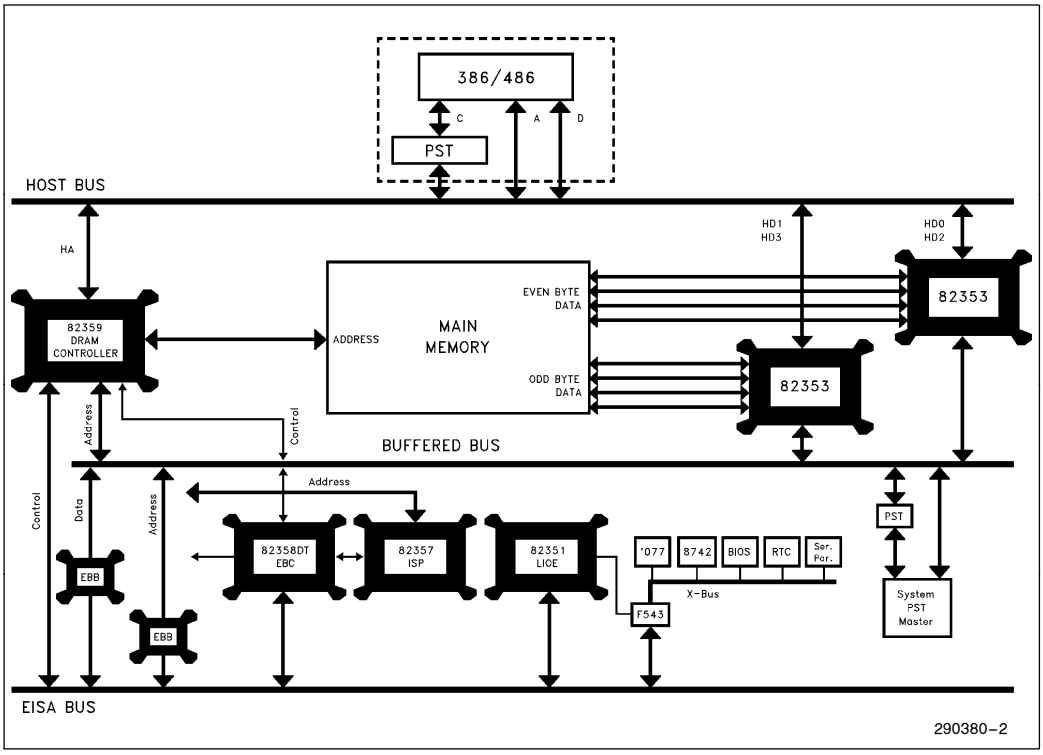


Figure 2-3. 82350DT System Environment (Buffered Configuration)

EISA operation is unchanged in the **82350DT/buffered** configuration. This configuration differs from the 82350DT/enhanced configuration in that a high speed bus (buffered bus) similar to the host bus has been added between the 82358DT and 82359. The buffered bus can be used by peripheral devices to access main memory at higher speeds than allowed on the EISA or ISA buses. This bus is transparent to the 82358DT. Peripheral devices located on this bus are treated as host devices.

2.2 82358DT Internal Architecture Overview

The following is a discussion of the major functional blocks internal to the EISA Bus Controller. Figure 2-4 shows these internal blocks.

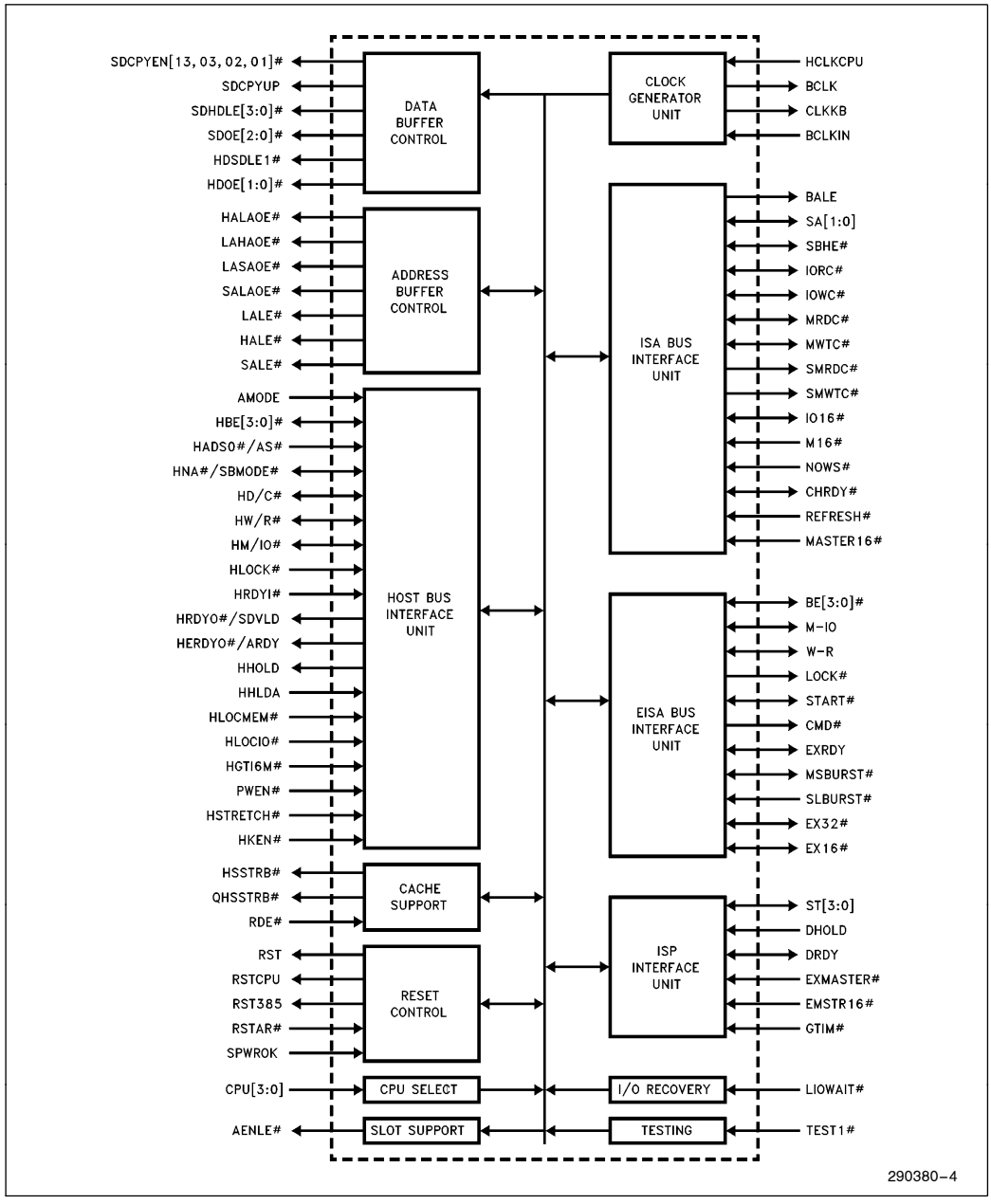


Figure 2-4. 82358DT Internal Block Diagram

2.2.1 HOST BUS INTERFACE UNIT

The host bus interface unit monitors cycles on the host bus. If no slave device on the host bus responds, and the cycle was initiated by a host master, then the 82358DT signals the EISA or ISA interface unit to run a cycle. The host bus interface unit waits for the EISA or ISA interface unit to complete the cycle, and then it terminates the cycle on the host bus.

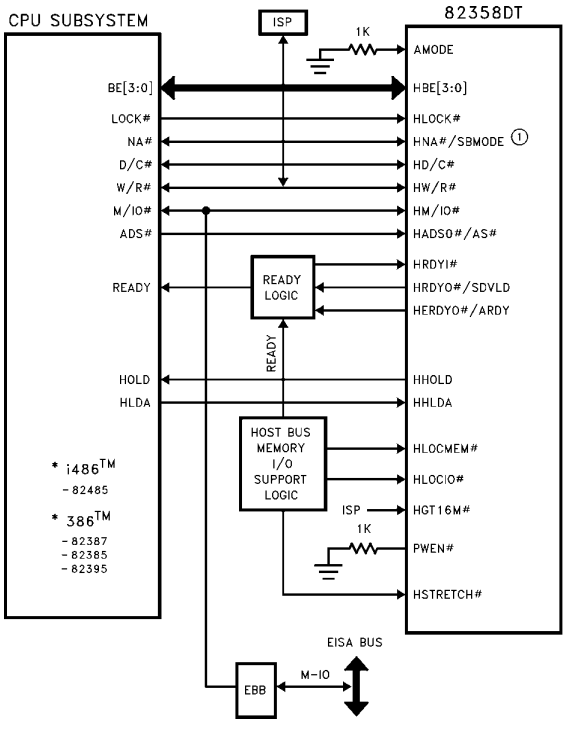
The host bus interface unit provides five mode/function select pins that allow the 82358DT to be strapped for either 82350 or 82350DT systems. Additional features selectable by these mode pins are posting of memory writes to the EISA/ISA bus. A complete description of these mode pins is provided in section 4.1.

The 82358DT multiplexes between the 82350 host interface and the 82350DT host interface based on the host configuration selected (82350 or 82350DT). Four host cycle control signals change in function based on this selection. These signals are referred to as the host multiplexed signal group and are shown in Table 2-1. The signals listed below are described in detail in the pin description section, section 3.1.1. Figures 2-5 through 2-7 illustrate the three basic host interface system interconnects.

Table 2-1. Host Multiplexed Signal Group

Pin #	Signal Name	82350 Compatible	82350DT Compatible
72	HADS0#/AS#	HADS0#	AS#
114	HERDYO#/ARDY	HERDYO#	ARDY
112	HRDYO#/SDVLD	HRDYO#	SDVLD
127	HRDYI#	HRDYI#	1 KΩ Pull-up

The host interface also provides a special protocol using the host bus signal HSTRETCH# that enables BCLK low time to be stretched in CLK1 increments. This allows slow host slave devices to use HSTRETCH# to run zero wait state EISA/ISA cycles (refer to section 4.9).



NOTE:
(1) In an i486 system, HNA# is defined as a ''no connect''. An internal pullup resistor is provided to insure that this signal is pulled high when tri-stated.

Figure 2-5. 82350 Host Interface

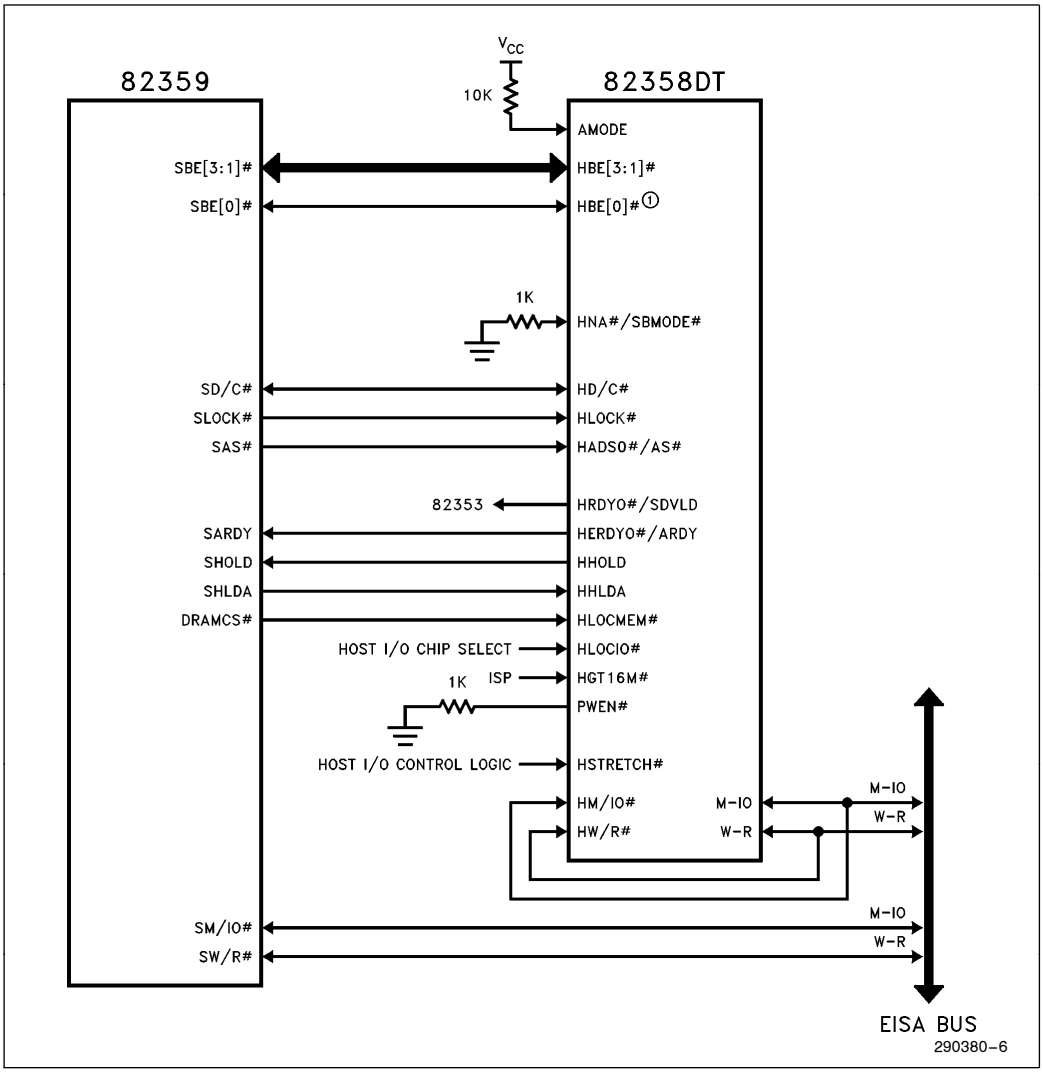


Figure 2-6. 82350DT/Enhanced Host Interface

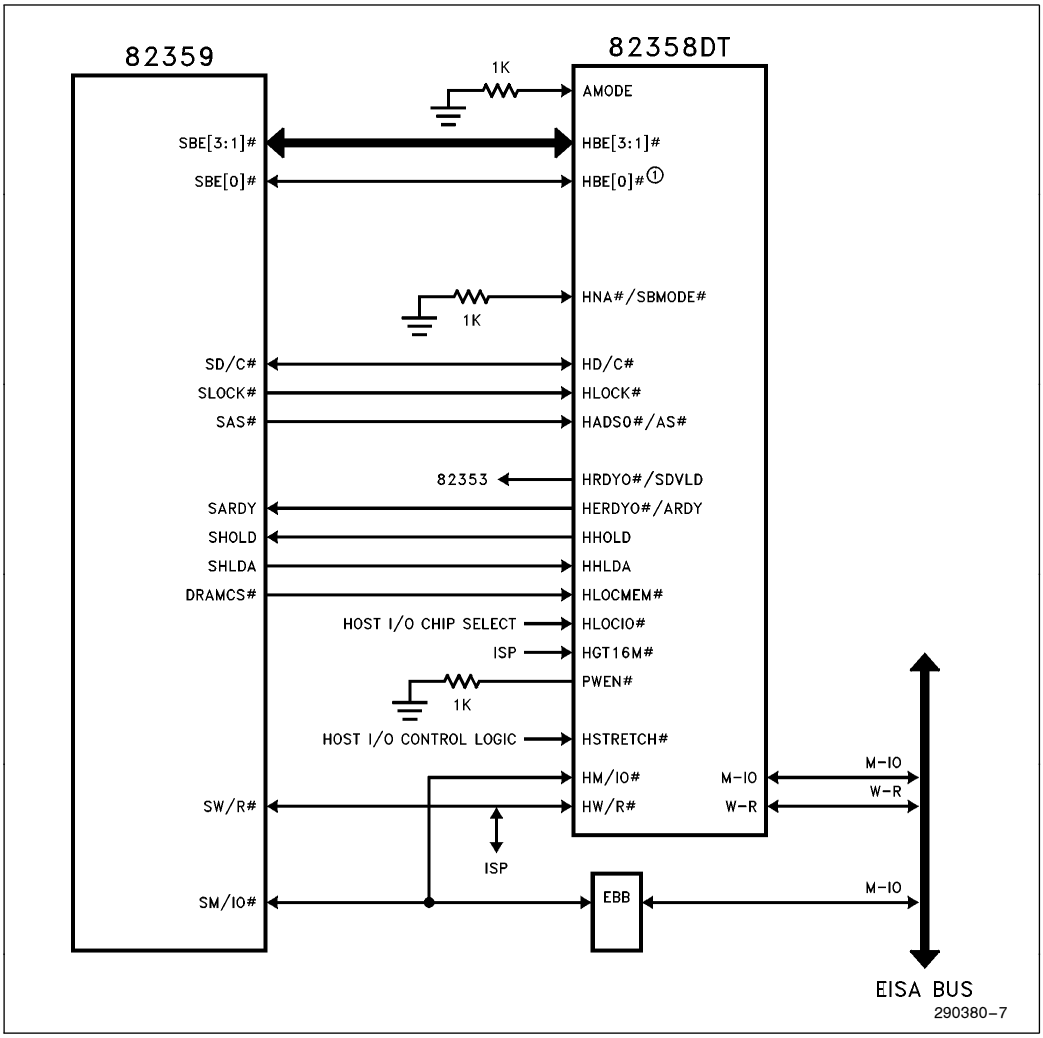


Figure 2-7. 82350DT/Buffered Host Interface

2.2.2 EISA AND ISA BUS INTERFACE UNITS

These state machine units interface to the EISA and ISA bus. They run at the EISA bus clock (BCLK) frequency.

The EISA unit interfaces to the EISA bus and executes EISA cycles on behalf of the ISA, host, and ISP interface units. In this way, any master can communicate with the EISA bus.

Similarly, the ISA unit interfaces to the ISA bus and executes ISA cycles on behalf of the EISA, host,and ISP interface units.

The EISA and ISA units, if necessary, will run multiple EISA or ISA cycles for data byte assembly/disassembly when the masters and slaves data sizes do not match.

The EISA and ISA interface units also accept requests from the ISP interface unit to run DMA cycles or refresh cycles on the EISA or ISA bus.

2.2.3 ISP INTERFACE UNIT

The ISP interface unit accepts requests from the ISP for DMA or refresh cycles, and then requests the ISA and EISA interface units to run the appropriate cycle. There are four types of DMA cycles: compatible, type A, type B, and type C (burst). If the memory slaves data size does not match the I/O slaves data size, the EISA/ISA interface unit will perform the byte assembly or disassembly as necessary through multiple EISA/ISA cycles.

2.2.4 DATA BUFFER CONTROL UNIT

This unit controls the data swap buffer/latch logic between the host, EISA, and ISA buses. It provides the latching clocks and the output enables for this logic. In an 82350, and an 82350DT/buffered system environment, this logic is implemented using an 82352 EBB (refer to Figures 2-1 and 2-3). In an 82350DT/enhanced system, this logic is implemented using two 82353 Advanced Data Buffers (refer to Figure 2-2).

The data buffer control unit interfaces with the host, EISA, and ISA interface units to provide external buffer control during assembly/disassembly of data, which allows copying of data between byte lanes.

2.2.5 ADDRESS BUFFER CONTROL UNIT

The address buffer control unit controls the external bi-directional address buffers (implemented using an 82352 EBB) between the host and EISA/ISA bus (refer to Figures 2-1 through 2-3). It provides the latching clocks and output enables for the EBB. In an 82350DT/enhanced system, the 82359 drives the host address directly to the EISA/ISA bus, bypassing the EBB. In this case, the address buffer control unit latches the EISA/ISA address via the 82359 DRAM controller on the rising edge of LALE#. LALE# is tied to IASALE# on the 82359.

2.2.6 CACHE SUPPORT UNIT

In an 82350/386/82385 system, the cache support logic instructs the 82385 cache controller when to snoop the system bus (HSSTRB#). HSSTRB# is a synchronized strobe indicating a valid address during host master, EISA master, ISA master, and DMA write cycles to system memory.

In 82350/i486 and 82350/386/82395 systems, the cache support logic instructs the i486 microprocessor and 82395 cache controller when to snoop the system bus (QHSSTRB#). QHSSTRB# is a synchronized strobe indicating a valid address during non-microprocessor memory write cycles to system memory. QHSSTRB# is qualified with HHLDA.

In 82350DT systems, the snoop strobe to the host microprocessor is generated by the 82359 DRAM controller. The 82358DT snoop strobes (HSSTRB# and QHSSTRB#) are defined as ''no connects'' when selected for 82350DT system environments.

In general, the cache support unit has the option (RDE#) to add a wait state by delaying HERDYO# and HRDYO# (82350 systems), or ARDY (82359DT systems) by one CLK1 during a host to EISA/ISA bus read to allow increased cache SRAM write data setup time during cache read miss cycles.

2.2.7 RESET CONTROL UNIT

This unit generates three types of resets:

1) *Reset for the CPU (RSTCPU)*

   This results under three conditions: during power-up, when shutdown is decoded, or when RSTAR# (restart) is asserted. The RSTCPU signal is interlocked with HHOLD such that only one of them will be active at a time, preventing CPU bus contention when the DMA or EISA/ISA bus master is active.

2) *Reset for the 82385 cache controller (RST385)*

   RST385 is asserted when RSTCPU is asserted, but delayed by 16 HCLKCPUs. RST385 is delayed so that the CPU completes its cycles before the 82385 is reset. This prevents the 82385 from erroneously glitching its BADS# output signal. For software resets (RSTAR# active) and shutdown cycles, RST385 active edge is delayed from RSTCPU active edge. For hardware resets (SPWROK active), the 82358DT generates RST385 and RSTCPU simultaneously.

3) *RESET for the ISP (RST)*

   This is generated at power-up after BCLK is stable.

2.2.8 I/O RECOVERY UNIT

This unit forces a delay between back-to-back 8-bit and 16-bit ISA I/O cycles originating on the host bus. A controlled delay is inserted depending on the state of the LIOWAIT# pin. If LIOWAIT# is sampled inactive, a minimum of one BCLK delay is added.If LIOWAIT# is sampled active, a maximum of three BCLKs for a 16-bit I/O or 11 BCLKs for an 8-bit I/O is inserted, depending on when LIOWAIT# is sampled inactive again. A complete description of this function is provided in section 4.10.

This unit is also responsible for inserting a one BCLK delay between the following cycles originating on the host bus: before an EISA or ISA I/O cycle following an ISA memory cycle, and before an EISA or ISA memory cycle following an ISA I/O cycle.

No delay is added, by the 82358DT, between any other back-to-back cycles.

2.2.9 SLOT SUPPORT UNIT

The slot support unit generates an address latch enable signal (AENLE#) for the purpose of generating the slot specific AENx# signals. A complete description of this function is provided in section 4.15.

2.2.10 CLOCK GENERATION UNIT

This unit generates three clocks:

1) **EBC__CLK1** (Host State Machine Clock) - This clock runs at the same frequency as the internal clock of the Host CPU. It is synchronized to the entire system board by SPWROK. In 80386 systems, EBC__CLK1 is generated internally from HCLKCPU divided by two. In i486 systems, EBC__CLK1 is an inverted version of HCLKCPU.
2) **BCLK** - This is the EISA clock that runs at approximately 8 MHz. It is generated by dividing HCLKCPU by 3, 4, 6, or 8, depending on the state of the CPU[3:0] signals. The CPU[3:0] signals indicate the CPU type and frequency. This unit also stretches the high or low time of BCLK for synchronization purposes (refer to section 4.9). In addition to being the synchronous clock source for the EISA bus, BCLK must also be tied to the 82358DT's BCLKIN input for internal synchronization purposes.
3) **CLKKB** - This is the clock for the keyboard processor. It is generated by dividing HCLKCPU by 3, 5, or 6, depending on the state of the CPU[3:0] signals.

3.0 82358 PIN DESCRIPTION

This section defines the functions of the 82358DT pins. All signal descriptions apply to both the 386 and i486 CPU, and the 82350 and 82350DT systems, unless otherwise stated. The symbol "#" after the signal name denotes active low.

3.1 Host Bus Interface Signals

3.1.1 MULTIPLEXED HOST INTERFACE SIGNAL GROUP

This signal group includes four multiplexed signals that change in function depending on the state of host interface mode select pin HNA#/SBMODE# during power-up. When operating in an 82350 system environment (SBMODE# = 1), the signals function as described in the pin descriptions for signals HADS0#, HERDYO#, HRDYO#, and HRDYI#. When operating in an 82350DT system environment (SBMODE# = 0), the signals function as described in the pin descriptions for signals AS#, ARDY and SDVLD. The multiplexed signals are shown in Table 3-1.

Table 3-1. Multiplexed Signal Group

Pin#	Signal Name	82350 Compatible	82350DT Compatible
72	HADS0#/AS#	HADS0#	AS#
114	HERDYO#/ARDY	HERDYO#	ARDY
112	HRDYO#/SDVLD	HRDYO#	SDVLD
127	HRDYI#	HRDYI#	1 KΩ Pull-Up

82350 Compatible

HOST ADDRESS STATUS INPUTS (HADS0# AND HADS1#)

The falling edge of HADS0# and HADS1# indicate that address, status, and byte enable information is valid on the host bus. In the case of pipelined cycles, HADS0# and HADS1# are expected to stay active low until HRDYI# has been sampled active by the 82358DT. These signals are received by the 82358DT when there is a master on the Host Bus, and are used to track the start of a host bus cycle. When no host slave responds, the cycle will be forwarded to the EISA bus (i.e., the CPU is addressing either an EISA slave, ISA slave, or the ISP).

HADS0# and HADS1# are internally "AND"ed together so that either one can signal the start of a cycle. These signals can be used for 64 K byte and 128 K byte cache designs where an independent state machine generates HADS1#. For example, 128 K byte 82385 cache systems use more than one fetch to fill a cache line. The 82385 starts the first cycle by generating HADS0# and the state machine completes any additional fetches by generating its own HADS1# signal. In the circuit, HADS0# connects to the 82385, and HADS1# connects to the state machine.

HOST BUS READY OUTPUT (HRDYO#)

HRDYO# is driven active for CPU master to EISA/ISA slaves, halt, shutdown, and ISP cycles. When the CPU is addressing an EISA/ISA slave or the ISP, this signal is driven active to indicate that the 82358DT has completed the cycle, as generated from EXRDY, CHRDY, NOWS#, DRDY, whichever is appropriate. In the next cycle, HRDYO# is driven inactive and then tri-stated. In the case of a posted write cycle, HRDYO# is driven active to terminate the host portion of the transfer. The EISA/ISA portion of the transfer is then completed and terminated in the normal manner. For halt and shutdown cycles, the 82358DT responds with a HRDYO# in zero CPU wait states (non-pipelined).

HOST BUS EARLY READY OUTPUT (HERDYO#)

This is an early version of the ready output from the 82358DT to be synchronized externally for use with higher frequency CPUs where HRDYO# does not provide adequate setup time. HERDYO# is driven active one CLK1 cycle earlier than HRDYO# except during CPU halt and shutdown cycles, in which case, HERDYO# is driven active concurrently with HRDYO#. The need for external synchronization for higher frequency CPUs could cause an extra wait state to be added for halt/shutdown cycles. Unlike HRDYO#, HERDYO# is not tri-stated after being driven inactive.

HOST BUS READY INPUT (HRDYI#)

HRDYI# is used by the 82358DT to track host master initiated cycles (Host to Host, Host to EISA, and Host to ISA slave cycles).

NOTE:
HRDYI# is not used during host master pipelined cycles to EISA or ISA slaves when ADS# for the second cycle occurs before CMD# rising of the first cycle.

When driven active, this signal indicates the termination of a cycle on the host bus. HRDYI# cannot be delayed by more than one CLK1 from HERDYO#.

82350DT Compatible

ADDRESS STROBE INPUT (AS#)

AS# is an asynchronous input to the 82358DT from the 82359 DRAM controller. The falling edge of AS# is synchronized to HCLKCPU. When driven active, AS# indicates to the 82358DT that the address is valid on the EISA/ISA bus and HM/IO#, HW/R#, HD/C#, and HBE[3:0]# are valid on the 82358DT host bus interface. If HLOCMEM# and HLOCIO# are sampled inactive, and a special cycle transfer is not indicated, AS# is used to initiate a host to EISA/ISA or host to ISP cycle. AS# stays active until after ARDY has been returned active (high) to the 82359 DRAM controller for a non-burst read and all write cycles. For host CPU burst read cycles (HBURST# sampled low), AS# stays active until after the last rising edge of SDVLD (as dictated by the burst count sampling of HBE[1:0]# at power-up).

ASYNCHRONOUS READY OUTPUT (ARDY)

ARDY is an input to the 82359 DRAM controller and used, when negated low, to indicate a *not ready* condition during host cycles to the EISA/ISA bus. The rising edge of ARDY indicates the end of the EISA/ISA or ISP cycle. ARDY is generated from either EXRDY, CHRDY, NOWS#, or DRDY, whichever is appropriate. This signal is driven low after AS# has been synchronized and HLOCMEM# and HLOCIO# have been sampled high for accesses to the EISA/ISA bus or special cycle transfers (i.e., halt, shutdown, flush, interrupt acknowledge cycles). ARDY is set high again when the EISA/ISA cycle is complete. For posted memory write cycles, the host bus portion of the cycle is terminated (ARDY driven active) after the host write data has been latched on the rising edge of HDSDLE1#.

SYSTEM DATA VALID OUTPUT (SDVLD)

SDVLD indicates to the 82353 (ADP) that valid read data is setup to its internal latches and can be frozen. For host cycles that require multiple EISA/ISA cycles for assembly, the falling edge of SDVLD occurs after the assembly process is complete. SDVLD is pulsed active just for Host master to EISA/ISA bus read cycles.

3.1.2 MODE SELECT HOST INTERFACE SIGNALS

The following five signals are used to select various modes and features available with the 82358DT. Three of the signals, HNA#/SBMODE#, HBE0#, and HBE1# have additional functions. The mode select signals are described below. For additional information not provided by the following pin descriptions, refer to section 4.1.

HOST NEXT ADDRESS/82350DT MODE I/O (HNA#/SBMODE#)

HNA#/SBMODE# provides two functions:

1) Mode Select Function Input (SBMODE#)

   As an input, HNA#/SBMODE# functions as a mode pin which allows the 82358DT to be selected for operation in either an 82350 or 82350DT system environment. Specifically, this signal selects between the 82350 host bus interface and the 82350DT host bus interface. When selected for an 82350 environment (HNA#/SBMODE# = 1), the 82350 host bus control signals **HADS0#, HERDY0#, HRDY0#** and **HRDYI#** are used. When selected for an 82350DT environment (HNA#/SBMODE# = 0), the 82350DT host bus control signals **AS#**, **ARDY**, and **SDVLD** are used.

   HNA#/SBMODE# is sampled on the rising edge of SPWROK to determine the mode of operation. This signal is an input during power up only, and must meet the setup and hold times T6c and T6d for proper operation. An internal pullup resister has been provided to insure that this signal defaults to 82350 mode when placed in an 82350 system environment. To select the 82358DT to operate in an 82350DT system environment, HNA#/SBMODE# can be strapped low with a 1K pulldown resister.

2) Host Next Address Output (HNA#)

   The second function provided by this pin applies when the 82358DT is used in an 82350/386 system environment.

   As an output, this signal indicates to the Host bus master that a new address can be placed on the bus for address pipelining purposes. HNA# is pulsed active for one host CLK1 period, indicating that the addressed EISA, ISA or ISP slave is ready for a new address. HNA# is active only during Host bus master cycles, and is tri-stated for all other cycles. An internal pullup resister is provided to insure that a high level is present when this signal is tri-stated. HNA# is defined as a ''No Connect'' pin when used in an 82350/i486 system. In an 82350DT system, HNA# floats and should be tied low with a 1K pulldown resistor. Refer to section 4.12 for a description on 82358DT address pipelining support.

POSTED WRITE ENABLE INPUT (PWEN#)

PWEN# is a dynamically sampled mode pin used to enable posting of memory write cycles to the EISA/ISA bus. In 82350 systems, PWEN# is sampled on the rising edge of HCLKCPU, two CLK1's after HADS# is driven active. In 82350DT systems, PWEN# is sampled on the rising edge of HCLKCPU, two CLK1's after AS# is driven active. When sampled low, posting is enabled, when sampled high, posting is disabled. This signal can also be strapped low with a 1K pulldown to enable continuous posting of memory writes. A complete description on posting memory write cycles is provided in section 4.1.3.

ADDRESS MODE INPUT (AMODE)

AMODE is used to select between buffered (AMODE = 0) and enhanced (AMODE = 1) address/status control. Buffered address/status control is selected when the 82358DT is used in an 82350, or an 82350DT/buffered system environment. Enhanced address/status control is selected when the 82358DT is used in an 82350DT/enhanced system environment. TIE AMODE either high with a 10K resistor or low with a 1K resistor, depending on the desired function (refer to Table 4-1).

HOST BYTE ENABLES I/O (HBE0#-HBE1#)

These signals are tri-stated when HHLDA is driven inactive. If HHLDA is high during power-up, these signals are driven off of the rising edge of SPWROK.

HBE0# and HBE1#, along with HBE2# and HBE3#, are also used during normal operation as host byte enable signals. Refer to the HBE[3:0]# pin description for a complete description of this function.

3.1.3 HOST INTERFACE SIGNALS (GENERAL)

HOST CPU CLOCK INPUT (HCLKCPU)

For 386 and i486 systems, HCLKCPU runs at the same frequency as the external clock of the Host CPU.

HOST BYTE ENABLE I/O (HBE[3:0]#)

HBE[3:0]# are the byte enable signals used to indicate active bytes during read and write cycles on the

host bus. HBE3# applies to bits 31-24 of the host data bus, HBE2# to bits 23-16, HBE1# to bits 15-8, and HBE0# to bits 7-0. HBE[3:0]# are inputs to the 82358DT when the Host bus master is addressing an EISA or ISA slave and are translated to BE[3:0]#, SBHE#, and SA[1:0]. HBE[3:0]# are outputs during all cycles except for host bus master cycles. During EISA bus master cycles and ISP DMA or refresh cycles, HBE[3:0]# are derived from BE[3:0]#. During ISA bus master cycles, HBE[3:0]# are derived from SBHE#, SA[1:0].

NOTE:
HBE[1:0]# have additional functions as described in sections 3.1.2 and 4.7.

HOST DATA OR CONTROL I/O (HD/C#)

This signal differentiates between data and control cycles. HD/C# is an input to the 82358DT when a host master is owner of the Host bus. It is used along with HM/IO# and HW/R# to decode halt/shutdown cycles, interrupt acknowledge, read/write, and memory/IO cycles. HD/C# is an output of the 82358DT when the ISP is performing DMA or refresh cycles, and during EISA/ISA bus master cycles. HD/C# is driven (high) whenever it is an output. Table 4-22 in section 4.17 shows how HD/C#, HM/IO#, and HW/R# are used to determine bus cycle definition.

HOST MEMORY OR IO I/O (HM/IO#)

HM/IO# differentiates between memory and IO cycles on the host bus. HM/IO# is also used to decode shutdown and interrupt acknowledge cycles as shown in Table 4-22.

In 82350, and 82350DT/buffered systems, the 82358DT and the address buffers (EBB) share the responsibility of driving HM/IO#. In 82350DT/enhanced systems, the 82359 DRAM controller drives HM/IO# directly to the EISA/ISA bus. A complete description on the relationship between HM/IO#, M-IO and the ISA M/IO command signals, is provided in section 4.8.

HOST WRITE OR READ I/O (HW/R#)

H/WR# differentiates between write and read cycles on the host bus. HW/R# is also used to decode shutdown and interrupt acknowledge cycles as shown in Table 4-22).

In 82350, and 82350DT/buffered systems, HW/R# is an input to the 82358DT when a Host bus master is addressing an EISA/ISA slave or when the ISP is performing DMA or refresh cycles. It is propagated to the EISA bus as W-R, and if necessary causes the appropriate ISA command. In 82350DT/Enhanced systems, the 82359 DRAM controller drives HW/R# directly to the EISA/ISA bus. A complete description on the relationship between HW/R#, W-R and the ISA W/R command signals, is provided in section 4.8.

HOST BUS LOCAL MEMORY INPUT (HLOCMEM#)

This signal indicates that a host bus memory slave has decoded the current address as its own. If HLOCMEM# is driven active during 82350 host master cycles, the 82358DT will not start a cycle on the EISA/ISA bus. However, if HLOCMEM# is driven active when the 82358DT is configured for a 82350DT system environment, AS# must be blocked from reaching the 82358DT to guarantee that no cycles are started on the EISA/ISA bus. During DMA cycles or EISA/ISA bus master memory cycles, HLOCMEM# is used by the 82358DT to determine if the memory address being accessed is on the host bus. For EISA master memory cycles, if HLOCMEM# is driven active, then EX32# will be driven active by the 82358DT. The 82358DT assumes that a slave residing on the host bus is 32-bits.

HOST BUS LOCAL INPUT (HLOCIO#)

This signal indicates that a host bus I/O slave has decoded the current address as its own. During EISA/ISA bus master I/O cycles, this signal is used by the 82358DT to determine if the I/O being accessed is on the host bus. If HLOCIO# is driven active during 82350 host master cycles, the 82358DT will not start a cycle on the EISA/ISA bus. However, if HLOCIO# is driven active when the 82358DT is configured for a 82350DT system environment, AS# must be blocked from reaching the 82358DT to guarantee that no cycles are started on the EISA/ISA bus. For EISA master I/O cycles, if HLOCIO# is driven active, then EX32# will also be driven active by the 82358DT. The 82358DT assumes that a slave residing on the host bus is 32-bits. For ISA bus master cycles, if HLOCIO# is driven active, then IO16# will be driven active. In this case, the 82358DT will perform word copying between the upper and lower bytes, if necessary (no assembly or disassembly is required).

HOST BUS STRETCH INPUT (HSTRETCH#)

This input can be used by host bus slaves during EISA bus master cycles or DMA cycles (only) to stretch the low part of BCLK during CMD#. This has the effect of stalling the master without adding BCLK wait states. If HSTRETCH# is sampled active, BCLK will remain low. It is then sampled at every other HCLKCPU rising edge for 386 systems (CLK1 intervals) and every HCLKCPU rising edge for 486 systems, until it is sampled inactive. When HSTRETCH# is sampled inactive, BCLK will then go high. The HSTRETCH# inactive edge must be set-up to the HCLKCPU rising edge where BCLK is to go high.

HSTRETCH# should not be driven active until CMD# is driven active, and should not remain active for more than 400ns. To prevent HSTRETCH# from being driven active while CMD# is inactive, gate HSTRETCH# with CMD# active. Refer to section 4.9 for additional information.

HOST BUS HOLD REQUEST OUTPUT (HHOLD)

This is the hold request to the host, and is driven active by the 82358DT when the ISP drives DHOLD active to indicate that an EISA/ISA bus master is requesting control of the bus, a DMA device requires service, or refresh is pending. HHOLD is synchronous to the host CPU's internal clock (HCLKCPU/2 for 386 and HCLKCPU for 486). At 33 MHz, external synchronization is required to meet the set-up and hold time requirements for a 33 MHz CPU. This signal is interlocked with RSTCPU such that only one of them will become active at a time. Also, if a posted write cycle is in progress, and the ISP drives DHOLD active, the 82358DT will not drive HHOLD active to the CPU until the posted write cycle is completed on the EISA/ISA bus. This prevents the ISP from giving the bus to another master before the 82358DT has completed the write cycle.

HOST HOLD ACKNOWLEDGE INPUT (HHLDA)

HHLDA is an input to the 82350DT and is synchronous to the host CPU's internal clock (HCLKCPU/2 for 386 and HCLKCPU for 486). This signal is driven active by the host master to indicate that it has relinquished control of the bus.

HOST BUS LOCK INPUT (HLOCK#)

This signal is driven active by the host bus master when a locked bus cycle is occurring on the Host bus. If the addressed device is on the EISA bus, HLOCK# is propagated as LOCK# on the EISA bus. HLOCK# must be sampled inactive before the 82358DT will drive LOCK# inactive on the EISA bus. A description on locked cycles is provided in section 4.13.

HOST SNOOP STROBE OUTPUT (HSSTRB#)

HSSTRB# is driven active during DMA memory write cycles, EISA/ISA bus master memory write cycles, and CPU memory write cycles. This signal indicates to the cache controller that a bus master is writing to memory. In 82350(386/82385) systems, the 82385 cache controller use HSSTRB# to maintain cache coherency with data stored in EISA/ISA or host memory. HSSTRB# is tied to SSTB# on the 82385. In 82350(i486), 82350(386/82395), and 82350DT systems, HSSTRB# is defined as a ''No Connect'' pin. Section 4.11 provides a detailed description on 82358DT snoop support.

QUALIFIED HOST SNOOP STROBE OUTPUT (QHSSTRB#)

QHSSTRB# is driven active by the 82358DT during DMA memory write cycles and EISA/ISA bus master memory write cycles only. QHSSTRB# differs from HSSTRB# in that QHSSTRB# is not generated during CPU memory write cycles. In 82350(i486) and 82350(386/82395) systems, the i486 microprocessor and 82395 cache controller use QHSSTRB# to maintain cache coherency. QHSSTRB# is tied to EADS# on the i486 CPU and SEADS# on the 82395. In 82350(386/82385) and 82350DT systems, QHSSTRB# is defined as a ''No Connect'' pin. Section 4.11 provides a detailed description on 82358DT snoop support.

HOST GREATER THAN 16 MEGABYTES INPUT (HGT16M#)

This signal indicates the address of the current cycle is greater than the range of 00000000h to 00FFFFFFh (16 Meg). The 82358DT uses HGT16M# during DMA compatible cycles to EISA memory slaves to determine whether or not to generate ISA memory command signals MRDC# and MWTC#. If the valid address is less than 16 Meg (HGT16M# = 1), MRDC# or MWTC# will be generated, otherwise, MRDC# and MWTC# will not be generated. MRDC# and MWTC# are generated in this case due to the fact that some DMA devices use ISA memory command signals to begin a cycle early. HGT16M# is driven by the ISP for all addresses above 16 Mbytes for DMA cycles only.

HOST CACHE ENABLE INPUT (HKEN#)

HKEN# is used in i486/82350 and 386/82395/82350 systems during host master memory read cycles to the EISA/ISA bus. It indicates that the current address is cacheable. If HKEN# is driven active, the 82358DT will ignore the HBE[3:0]# value on the host bus and assume that all four byte lanes are requested (i.e., the 82358DT will drive BE[3:0]#

on the EISA bus active regardless of the state of the HBE[3:0]# signals). This signal is derived from the external cacheability map logic and is used during memory read cycles only. In an 82350DT system, HKEN# should be pulled high with a 10K pullup resistor (the 82359 automatically drives HBE#[3:0] low during a cacheable cycle).

3.2 EISA Bus Interface Signals

BYTE ENABLES I/O (BE3#-BE0#)

These signals indicate which bytes on the 32-bit EISA data bus are involved in the current cycle. BE3# corresponds to bits 24-31 of the EISA data bus, BE2# corresponds to bits 16-23, BE1# corresponds to bits 8-15, and BE0# corresponds to bits 0-7. BE[3:0]# are pipelined from one cycle to the next and must be latched by the EISA slave. During standard cycles, they are valid before BALE goes active and remain valid as long as the LA(31:2) address lines remain valid.

BE[3:0]# are outputs during host master cycles, ISA master cycles (excluding ISA master refresh cycles), EISA master cycles (during the assembly/disassembly portion of the cycle), and DMA cycles (during the assembly/disassembly portion of the cycle). During host master cycles not requiring assembly or disassembly, BE[3:0]# are derived combinatorially from HBE[3:0]# after the first falling edge of BCLK during CMD# of the previous cycle, except in i486 and 386/82395 systems when HKEN# is active, in which case BE[3:0]# are forced to 0000. During host master, EISA master, and DMA cycles where assembly or disassembly is required, BE[3:0]# are derived internally by the 82358DT. During non-refresh ISA master cycles, BE[3:0]# are derived combinatorially from SA[1:0] and SBHE#.

BE[3:0]# are inputs during EISA bus master cycles or when the ISP is performing DMA or refresh cycles. BE[3:0]# are translated to HBE[3:0]#, SA0, SA1, and SBHE#. Section 4.7 provides a translation table for BE[3:0]#, SA1, SA0, and SBHE#.

MEMORY OR I/O CYCLE OUTPUT (M-IO)

This signal is used to differentiate between memory cycles (high) and I/O cycles (low) on the EISA bus. It is driven during ISA master cycles, and is driven low if IORC# or IOWC# are driven active. M-IO stays low as long as IORC# or IOWC# are active. M-IO is floated during ISA master refresh cycles. M-IO is pipelined from one cycle to the next, and must be latched by the slave. A complete description on the relationship between M-IO, HM/IO# and the ISA M/IO command signals, is provided in section 4.8.

WRITE OR READ CYCLE I/O (W-R)

W-R is used to differentiate between read (low) and write (high) cycles on the EISA bus. W-R is pipelined from one cycle to the next, and must be latched by the slave. A complete description on the relationship between W-R, HW/R#, and the ISA W/R command signals, is provided in section 4.8.

START CYCLE I/O (START#)

START# provides timing control at the start of the cycle and remains active for one BCLK period. START# is an input to the 82358DT during EISA bus master cycles. START# is an output for all cycles except EISA master cycles, with the exception of EISA master to mismatched slave operations. In this case, START# becomes an output at the end of the first START# and remains as an output until the negation of the last CMD# (refer to section 4.5). During host master cycles, START# is generated in response to the beginning of a cycle on the host bus to which no host slave responded. START# is driven active after the address LA(31:2) and M-IO have become valid.

The falling edge of START# is delayed from the rising edge of BCLK except during host master and ISA master cycles where BCLK stretching is required (refer to section 4.9). The trailing edge of START# is always delayed from the rising edge of BCLK.

COMMAND OUTPUT (CMD#)

This signal provides timing control within the cycle. It is driven active from the rising edge of BCLK simultaneously with the negation of START#, and remains asserted until the end of the cycle. It is generated by the 82358DT for all cycles, except host to host and ISA master to ISA memory cycles. It is also driven active for ISA I/O cycles (for a possible ISP access). CMD# is driven inactive from the rising edge of BCLK, except as indicated in Table 3-2. During ISA master read cycles, CMD# is driven inactive asynchronously from the trailing edge of the ISA read command signals (IORC# and MRDC#). **NOTE:** Bus masters do not drive CMD#.

Table 3-2. CMD# Driven Inactive

Cycle Type	Driven Inactive
General Case	BCLK Rising
DMA Compatible Memory Read (Memory size GE I/O size)	BCLK Falling
Type ''A'' Memory Read (Memory size GE I/O size)	BCLK Falling
Type ''B'' Memory Read (Memory size GE I/O size)	BCLK Falling
Type ''C'' Memory Read Burst Back-off (Memory size GE I/O size)	BCLK Falling
ISA Master Read Cycle (Memory Read or I/O Read)	IORC# or MRDC#

GE = Greater Than or Equal To

MASTER BURST I/O (MSBURST#)

As an input, this signal is used to indicate that the current EISA bus master is capable of supporting the next cycle as a burst cycle. MSBURST# is sampled on the rising edge of BCLK after the rising edge of BCLK that CMD# is driven active. MSBURST# is sampled on all subsequent rising edges of BCLK until sampled inactive. The burst cycle is terminated on the rising edge of BCLK that MSBURST# is sampled inactive, unless EXRDY is sampled inactive on the previous falling edge of BCLK. In this case, CMD# will remain active until EXRDY is sampled active.

This signal is an output during DMA burst cycles. MSBURST# is driven active on the falling edge of BCLK, one half of BCLK after SLBURST# is sampled active and remains active until the falling edge of BCLK that a change in the status signals, ST[3:0], is detected (refer to Figures 5-62 through 5-64). MSBURST# is sampled by memory slaves on the rising edge of BCLK.

SLAVE BURST INPUT (SLBURST#)

This signal is driven active by EISA memory slaves to indicate that they are capable of accepting burst cycles. SLBURST# is sampled on the rising edge of BCLK, one BCLK after the ST[3:0] lines are sampled active for DMA cycles. SLBURST# is sampled on the rising edge of BCLK at the end of START# for EISA Master cycles. Please refer to Figures 5-62 through 5-65.

16-BIT MASTER INPUT (MASTER16#)

This signal indicates a 16-bit EISA or ISA master has control of the EISA bus. The 82358DT samples MASTER16# on the rising edge of BCLK that START# is driven active. If MASTER16# is sampled active at this sampling point, no additional sampling is done. At this time, the 82358DT identifies the master as either a 16-bit EISA or ISA master. If MASTER16# is sampled inactive at the beginning of START#, the 82358DT will sample it a second time on the rising edge of BCLK at the end of START#. If MASTER16# is sampled active at the second sampling point, a 16- bit EISA master that has downshifted from a 32-bit EISA master is indicated. At this time, the 82358DT will disable automatic 32- to 16-bit data size translation. The downshifted master may then perform burst cycles to a 16-bit EISA slave. If MASTER16# is sampled inactive at both sampling points, a master other than a 16-bit EISA or ISA master is indicated.

EISA 32-BIT DEVICE I/O OPEN COLLECTOR (EX32#)

As an input, this signal is driven active by 32-bit EISA slaves to indicate their 32-bit data bus size. The 82358DT uses this signal as part of its slave decode to determine if data size translation and/or cycle translation is required (refer to Table 4-8). EX32# is also sampled one CLK1 after MRDC# or MWTC# is driven active during ISA master to host memory transfers to determine if EISA cycles should be generated.

As an output, if the master and slave data sizes are mismatched, and the master is a 16 or 32-bit EISA master, then the 82358DT will drive EX32# active to indicate completion of the data translation. This is required during master back-off to notify the master that cycle control is now returned (refer to section 4.5). The 82358DT will also drive EX32# active during 16 and 32-bit EISA master I/O and memory cycles to the host bus if either HLOCIO# or HLOCMEM# are driven active.

EISA 16-BIT DEVICE I/O OPEN COLLECTOR (EX16#)

As an input, this signal is driven active by 16-bit EISA slaves to indicate their 16-bit data bus size. The 82358DT uses this signal as part of its slave decode to determine if data size translation and/or cycle translation is required (refer to Table 4-8).

As an output, if the master and slave data sizes are mismatched, and the master is a 16 or 32-bit EISA master, then the 82358DT will drive EX16# active to indicate completion of the data translation. This is required during master back-off to notify the master that cycle control is now returned (refer to section 4.5).

EISA READY INPUT (EXRDY)

EISA memory and I/O slaves drive EXRDY inactive to add wait states (each wait state is one BCLK). EXRDY is an input during host master cycles to the EISA/ISA bus, EISA and ISA bus master cycles, and DMA cycles when an EISA slave responds with EX16# or EX32# asserted (refer to Table 3-4). EXRDY is sampled on the falling edge of BCLK after CMD# has been driven active (except during DMA compatible cycles), and if inactive, each falling edge thereafter. During DMA compatible cycles, EXRDY is sampled on the second falling edge of BCLK after CMD# is driven active, and if inactive, each falling edge thereafter CMD# remains active for the entire period that EXRDY is negated, and at least half a BCLK after EXRDY is sampled active. EXRDY is translated to HERDYO#, HRDYO# and ARDY during host master cycles to EISA slaves; DRDY during DMA cycles that include EISA slaves; and CHRDY during ISA master cycles to EISA slaves.

As an output, EXRDY is forced low for one BCLK at the start of a potential DMA burst write cycle to insure that the initial write data is held long enough to be sampled by the memory slave (refer to Figures 5-63 and 5-65).

LOCKED CYCLE OUTPUT (LOCK#)

This signal is driven active by the 82358DT when the host master is running locked cycles to EISA slaves. This guarantees exclusive memory access during the time LOCK# is active. A complete description on locked cycles is provided in section 4.13.

3.3 ISA Bus Interface Signals

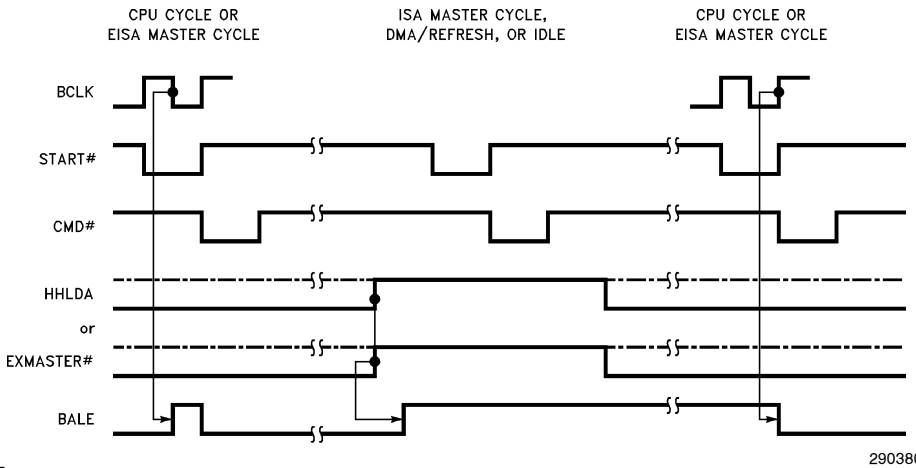
BUS ADDRESS LATCH ENABLE OUTPUT (BALE)

This signal is driven active to indicate that a valid address is present on the LA address bus. ISA slaves should use the falling edge of BALE to latch the LA bus.

During host and EISA master cycles, BALE is driven active on the falling edge of BCLK during START#. BALE will remain active until the same rising edge of BCLK that START# is negated (i.e. for one half of BCLK). If BCLK is stretched such that the falling edge of BCLK does not occur during START#, BALE will be driven active from the falling edge of START# and remain active for one BCLK (refer to Figure 4-18). In the case of an ISA master, DMA, or Refresh cycle preceding either a host master or EISA master cycle, BALE will be active coming into the cycle and will be driven inactive as mentioned above (i.e. on the rising edge of BCLK that START# is negated).

During ISA master, DMA, and Refresh cycles, BALE is driven active combinatorially with HHLDA high and EXMASTER# high, and will remain active throughout the entire cycle. BALE will not be negated again until the rising edge of BCLK that START# is negated during either a host or EISA master cycle.

Figure 3-1 shows the timing for BALE during Host, EISA, ISA, and DMA cycles.



NOTE:
The rising edge of BALE is delayed from HCLKCPU rising at START# active, during host master cycles when BCLK is stretched.

Figure 3-1. BALE Timing

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BUS CLOCK OUTPUT (BCLKOUT)

BCLKOUT is the system clock used to synchronize events on the EISA/ISA bus. The 82358DT divides the HCLKCPU by a divisor based on how CPU[3:0] are strapped, to generate BCLKOUT (refer to Table 3-3). The maximum frequency is 8.333 MHz with a normal duty cycle of 50%. The high or low time of BCLKOUT can be stretched as shown in section 4.9.

Table 3-3. BCLKOUT Generation from HCLKCPU

CPU[3:0]	HCLKCPU Divided by
1010 - 25 MHz 80386	/6
1011 - 33 MHz 80386	/8
1100 - 25 MHz 80486	/3
1101 - 33 MHz 80486	/4

NOTE:
All other bit combinations are reserved.

I/O READ CONTROL STROBE I/O (IORC#)

This is the command to an ISA I/O slave that it may drive data to the data bus. IORC# is an output signal for all cycles, except during ISA master cycles. The 82358DT drives IORC# active when a host master or EISA master is addressing an ISA I/O slave, and during DMA memory write cycles. IORC# is an input during ISA master cycles and is translated to EISA control signals.

I/O WRITE CONTROL STROBE I/O (IOWC#)

This is the command to an ISA I/O slave that it may latch data from the data bus. The 82358DT drives IOWC# active when the CPU or an EISA master is addressing an ISA I/O slave, and during memory read DMA cycles. IOWC# is an input during ISA master cycles and is translated to EISA control signals.

INPUT/OUTPUT 16-BIT I/O OPEN COLLECTOR (IO16#)

16-bit ISA I/O slaves decode SA(15:1) on the ISA bus without regard to IORC# or IOWC#, and drive IO16# active indicating that they are capable of performing 16-bit transfers. IO16# is sampled on the second falling edge of BCLK after CMD# is driven active. If IO16# is sampled active, CMD# will be driven inactive on the next rising edge of BCLK, indicating a 16-bit ISA I/O slave. If sampled inactive, the 82358DT will sample IO16# on every falling edge of BCLK until IO16# is sampled active (at which time CMD# will be driven inactive on the next rising edge of BCLK) or the cycle is completed (CMD# driven inactive), whichever occurs first. As an output, the 82358DT drives IO16# during ISA master cycles when a host I/O slave has responded with HLOCIO#. EISA slaves that support ISA bus masters must assert IO16# as well as EX32# (or EX16#) when addressed.

MEMORY READ CONTROL STROBE I/O (MRDC#)

This is the command to an ISA memory slave that it may drive data to the data bus. MRDC# is an output when the CPU, an EISA master, or DMA is performing a memory read cycle to which neither host bus memory nor EISA memory responded. During memory read compatible DMA cycles, MRDC# is driven active in all cases, except when a 16-bit or 32-bit EISA memory, or host memory responds and the address is above the range of 00000000h to 00FFFFFFh (HGT16M# has been driven active). MRDC# is also an output during all refresh cycles (i.e. ISP or ISA master initiated refresh cycles). MRDC# is an input during ISA master cycles and is translated to EISA control signals.

MEMORY WRITE CONTROL STROBE I/O (MWTC#)

This is the command to an ISA memory slave that it may latch data from the data bus. The 82358DT drives MWTC# active when the CPU, EISA master, or DMA is performing a memory write cycle to which neither host bus memory nor EISA memory responded. During memory write compatible DMA cycles, MWTC# is driven active in all cases, except when an EISA memory responds and the address is above the range of 00000000h to 00FFFFFFh (HGT16M# has been driven active). MWTC# is an input during ISA master cycles and is translated to EISA control signals.

16-BIT MEMORY INPUT (M16#)

This signal indicates to the 82358DT that the addressed ISA memory is capable of performing 16-bit transfers. This signal is sampled twice by the 82358DT: once at the end of START# on the rising edge BCLK, and a second time on the falling edge of BCLK, one half a BCLK after START# is negated. The 82358DT uses the first sampling point to determine whether to delay the ISA cycle commands. The ISA commands are delayed by one half of BCLK if M16# is sampled negated at this first sampling point. The second sampling point is used to determine the slave size. If M16# is sampled active at the

second sampling point, a 16-bit memory slave is indicated, otherwise an 8-bit slave is indicated. Table 4-8 shows M16# decode for slave size determination.

STANDARD MEMORY READ CONTROL STROBE OUTPUT (SMRDC#)

This signal is the command to an ISA memory slave that it may drive data to the data bus. The 82358DT drives SMRDC# active during CPU, DMA, Refresh, and EISA/ISA master read cycles to 8 and 16-bit ISA memory slaves if the address is within the range 00000000h to 000FFFFFh (GT1M# is inactive). SMRDC# has similar timings as MRDC#. SMRDC# is floated by the 82358DT during the time GT1M# is active. A pullup resistor is required on SMRDC# to maintain an inactive state during this time.

STANDARD MEMORY WRITE CONTROL STROBE OUTPUT (SMWTC#)

This is the command to an ISA memory slave that it may latch data from the data bus. The 82358DT drives SMWTC# active whenever it drives MWTC# active, and the address is within the range 00000000h to 0000FFFFFh (GT1M# is inactive). SMWTC# has similar timings as MWTC# The 82358DT floats SMWTC# during the time GT1M# is active. A pullup resistor is required on SMRDC# to maintain an inactive state during this time.

Channel READY I/O OPEN COLLECTOR (CHRDY)

CHRDY is used by ISA slaves to insert wait states. Wait states are added if CHRDY is negated (low). As an input, the falling edge of CHRDY is captured asynchronously by the 82358DT. The 82358DT stops adding wait states on the rising edge of BCLK after the rising edge of BCLK that CHRDY is sampled asserted (high), except during compatible DMA cycles, in which case the cycle is terminated three to three and half BCLKs after the assertion of CHRDY, depending if CMD# is driven inactive on the rising or falling edge of BCLK (refer to the CMD# pin description and Figure 5-49). The ISA command signals will remain active at least one BCLK after CHRDY is sampled high. The 82358DT samples CHRDY during host master and EISA bus master cycles to ISA slaves, and during DMA accesses to ISA memory. CHRDY takes precedence over NOWS# (i.e., if CHRDY is inactive (low), NOWS# driven active is ignored). CHRDY also takes precedence over IO16# when IO16# is used to shorten the cycle. CHRDY is translated and used to generate HRDYO# and HERDYO#, ARDY, EXRDY, or DRDY, depending on the master in control of the bus and the system environment (82350, 82350DT/enhanced, or 82350DT/buffered).

CHRDY is an output during all ISA master cycles, except cycles to ISA memory, and is driven inactive (low) from the ISA command signals. During an ISA master cycle to a Host, EISA (excluding 8-bit EISA slaves), or ISA (16-bit ISA I/O only) slave, the EBC floats CHRDY from the first falling edge of BCLK in CMD# active, unless EXRDY or DRDY is sampled inactive (low). In this case, the EBC will float CHRDY from the falling edge of BCLK that EXRDY and DRDY are sampled active (high) again. During cycles to 8-bit EISA and ISA I/O slaves, the EBC will float CHRDY from the falling edge of BCLK, 4.5 BCLK's after START# is driven inactive, again unless EXRDY or DRDY is sampled inactive. Table 3-4 below shows CHRDY and EXRDY functional descriptions, and Figure 3-2 shows CHRDY functionality for ISA master cycles.

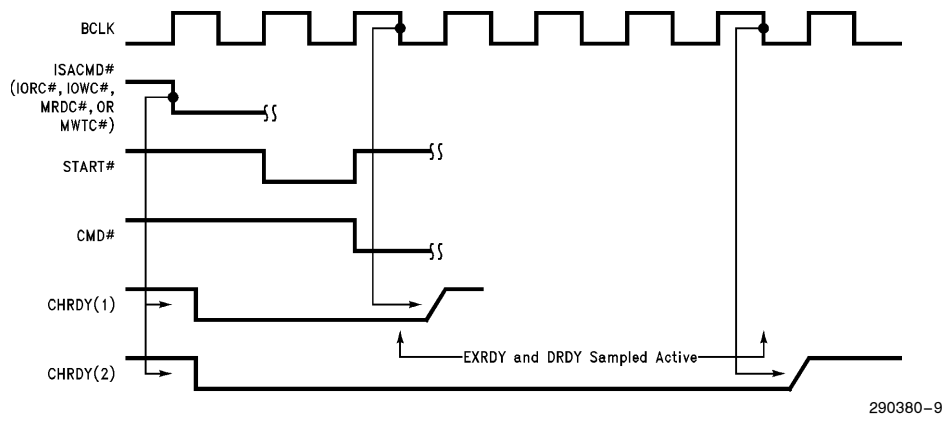
Table 3-4. CHRDY and EXRDY Functional Description

Master	EXRDY	CHRDY
CPU/EISA	INPUT(1)	INPUT(1)
DMA	I/O(2)	INPUT(1)
ISA	INPUT	OUTPUT(3)

NOTES:
1. CHRDY is driven by ISA slaves and EXRDY is driven by EISA slaves.
2. The 82358DT drives EXRDY inactive, as shown in Figures 5-63 and 5-65, during potential DMA burst write cycles. EXRDY is then placed in input mode.
3. Except ISA master to ISA memory cycles or ISA master to 8-bit EISA memory cycles.

NO WAIT STATES INPUT (NOWS#)

An ISA slave asserts NOWS# after its address and command signal have been decoded to indicate that the remaining clock cycles are not required. In order to shorten the cycle, NOWS# must be active at the falling edge of BCLK during CMD# active. The 82358DT will shorten the cycle a maximum BCLK count (depending on the cycle type) as shown in Table 4-6. By driving NOWS# active on the appropriate falling edge of BCLK, a cycle clock count between the standard cycle length and the minimum cycle length can be obtained. If CHRDY and NOWS# are driven low during the same cycle, NOWS# will not be used and wait states will be added as a function of CHRDY. DMA cycles can not be shorten with NOWS# driven active, except during the subsequent cycles of an assembly or disassembly transfer, and only if the memory is ISA memory. The cycles are shorten as indicated for ISA memory slaves in Table 4-6.



NOTES:
1. CHRDY Case for ISA Master to Host, EISA (excluding 8-bit EISA slaves), and ISA (16-bit ISA I/O only) slaves.
2. CHRDY Case for ISA Master to EISA and 8-bit ISA I/O slaves.

Figure 3-2. CHRDY during ISA Master Cycles

SYSTEM ADDRESS BITS 1 & 0 I/O (SA1, SA0)

SA0 and SA1 are the least significant bits of the latched EISA address bus. They are inputs to the 82358DT during ISA master cycles, excluding ISA master refresh cycles, and are used to generate BE[3:0]# on the EISA bus and HBE[3:0]# on the host bus (refer to section 4.7). They are outputs of the 82358DT during host accesses to EISA/ISA slaves, and are derived from HBE[3:0]#. They are outputs during EISA master cycles to ISA slaves and DMA accesses to ISA memory, and are derived from BE[3:0]#.

SYSTEM BYTE HIGH ENABLE I/O (SBHE#)

When active, SBHE# indicates that the high byte on the ISA data bus (SD[15:8]) is valid. SBHE# is an input during ISA master cycles, except during ISA master refresh cycles, and is used to generate BE[3:0]# on the EISA bus and HBE[3:0]# on the host bus. SBHE# is an output during host accesses to EISA/ISA slaves and is derived from HBE[3:0]#. SBHE# is an output during EISA master cycles to ISA slaves, and DMA accesses to ISA memory in which case SBHE# is derived from BE[3:0]#. Refer to section 4.7 for additional information regarding SBHE# translations.

REFRESH INPUT (REFRESH#)

REFRESH# indicates the ISP is performing a refresh cycle. During refresh, the 82358DT generates MRDC# and CMD# signals to refresh the entire system memory.

3.4 ISP Device Interface Signals

ISP HOLD REQUEST INPUT (DHOLD)

The ISP drives DHOLD active to request the host bus on behalf of ISA/EISA masters, or when a DMA device requests service. DHOLD is used to generate HHOLD.

ISP READY I/O (DRDY)

DRDY indicates the end of the cycle. It is an input to the 82358DT when the ISP is in slave mode. During ISA bus master I/O cycles, CHRDY is driven inactive asynchronously, and is kept inactive until DRDY is sampled active at the falling edge of BCLK during CMD# active. DRDY is an output of the 82358DT during DMA and refresh cycles and has two functions: Two BCLK's after ST3 and ST2 go to their non-idle state, DRDY will be driven active (high) to the ISP indicating address pipelining on the host bus. After this, DRDY is the indication of the end of the current transfer, until ST3 and ST2 are driven to their idle state again. After ST3 and ST2 are driven to their idle state, DRDY may still be inactive for the last transfer (burst cycles only). Pipelining is stopped at page breaks or at the end of the transfer. This signal must be tied high with a 2.4K pullup resistor.

GREATER THAN 1 MEGABYTE INPUT (GT1M#)

This input indicates to the 82358DT that the current address is above the range from 00000000h to 000FFFFFh (1 Mbyte). The 82358DT uses GT1M# to determine if ISA commands SMRDC# and SMWTC# should be generated during an ISA memory cycle. If GT1M# is inactive during a host master, EISA/ISA bus master, or DMA cycle to an ISA memory slave, the 82358DT will generate either SMRDC# or SMWTC#, depending on the direction of the memory cycle (i.e., read or write). The ISP generates GT1M# for all cycles (DMA and non-DMA).

DMA STATUS I/O (ST3-ST0)

ST0 through ST3 are inputs during DMA and refresh cycles. They indicate what type of timing has been programmed for the current cycle, and the size of the I/O device involved in the DMA transfer. The 82358DT will generate the appropriate command signals for the ISP and will control the timing of the cycle. If the memory which responded does not match the size of the I/O device, and compatible timing has not been selected, the 82358DT will perform assembly or disassembly of data and use EISA/ISA timing. Table 3-5 shows the ST[3:0] decodes. ST[3:0] are sampled on the rising edge of BCLK.

NOTE:
During refresh cycles, ST3 and ST2 follow the 8-bit cycle definition, and ST1 and ST0 are undefined (i.e., 00XX).

Table 3-5. ST[3:0] Decode

ST[3:0]	I/O Device Type & Programmed Timing	Note
0000	8-Bit Device & Compatible Timing	A
0001	8-Bit Device & Type A Timing	B
0010	8-Bit Device & Type B Timing	B
0011	8-Bit Device & Type C (Burst) Timing	C
0100	16-Bit Device & Compatible Timing	A
0101	16-Bit Device & Type A Timing	B
0110	16-Bit Device & Type B Timing	B
0111	16-Bit Device & Type C (Burst) Timing	C
1000	32-Bit Device & Compatible Timing	A
1001	32-Bit Device & Type A Timing	B
1010	32-Bit Device & Type B Timing	B
1011	32-Bit Device & Type C (Burst) Timing	C
11XX	No Operation	

NOTES:
A. The 82358DT does not assembly or disassemble.
B. Type A/B. If the DMA is performing Type A/B transfers and the 82358DT needs to translate to ISA memory cycles (ISA memory slave), or assembly/disassembly is required, then the cycle reverts to memory timings similar to that used with EISA bus masters. The MRDC# and MWTC# signals are not active unless the system must do assembly/disassembly for ISA memory.
C. Burst cycles. If the DMA is performing a burst transfer and the memory does not support bursting (SLBURST# sampled inactive), the cycle reverts to memory timings similar to the standard memory cycle generated by EISA bus masters.

During cycles where the ISP is not the master, ST0 through ST3 pins are outputs and have the following functions:

ST0 has the ADS# function, it is the address strobe for the ISP. The ISP uses ST0 to latch the address (HA[15:2]), ST1 (M-IO), and HW/R# information. The ISP latches this information on the rising edge of ST0. For CPU cycles, ST0 will be active low for one host CLK1 in the beginning of START#; for EISA cycles, ST0 will be active during START#; and for ISA cycles, it will be driven low continuously.

ST1 is the M/IO function (1 = Memory cycle, 0 = IO cycle). It is derived from HM/IO# during CPU cycles to the EISA bus, and from M-IO during EISA bus master cycles.

ST2 is the INTA# function, which is active (low) when the 82358DT decodes an interrupt acknowledge cycle. An interrupt acknowledge cycle will result in a START-CMD sequence. This signal must be tied high with a 1.2 K pullup resistor.

ST3 is the cycle in progress (CIP#) function. This signal is an indication to the ISP system arbiter that there is a bus cycle in progress. It is used to detect when the EISA master has given up the bus after deasserting MREQ#. ST3 driven inactive at the end of the last assembly/disassembly cycle.

EISA MASTER INPUT (EXMASTER#)

This input signal indicates a 16 or 32-bit EISA master has control of the EISA bus. It is used by the 82358DT in conjunction with MASTER16#, to distinguish between 32-bit EISA masters, 16-bit EISA masters, and 16-bit ISA masters (refer to Table 4-7).

EARLY INDICATION OF 16-BIT ISA MASTER INPUT (EMSTR16#)

This signal from the ISP indicates a 16-bit ISA master is in control, or about to assume control. It gives the 82358DT enough time to be able to switch the direction of the control signals and the address buffers between the host bus and the EISA bus, when changing from host initiated cycles to ISA master initiated cycles.

3.5 Data Buffer Control Signals

COPY ENABLE OUTPUTS (SDCPYEN01#,02#,03#, and 13#)

These signals enable the byte copy operations between data byte lanes 0, 1, 2, and 3, as shown in Table 3-6.

Table 3-6. Copy Operations

Signal	Copy between Byte Lanes
SDCPYEN01#	0 (bits 0-7) and 1 (bits 8-15)
SDCPYEN02#	0 (bits 0-7) and 2 (bits 16-23)
SDCPYEN03#	0 (bits 0-7) and 3 (bits 24-31)
SDCPYEN13#	1 (bits 8-15) and 3 (bits 24-31)

SYSTEM (EISA/ISA) DATA COPY-UP OUTPUT (SDCPYUP)

SDCPYUP controls the direction of the byte copy operation. When active, the lower bytes are copied on to the higher bytes (copy-up). The direction is reversed (copy-down) when this signal is inactive. Copying of data bytes is done when the data bus size of the master and slave do not match.

HOST DATA TO SYSTEM (EISA/ISA) DATA LATCH ENABLE OUTPUT (HDSDLE1#)

This signal latches the data from the host data bus into the data swap byte latches. The data is then available to be driven onto the EISA data bus. HDSDLE1# controls the latching of host data bus bits 0- 31. This signal is used to latch the data onto the EISA/ISA bus during host master write cycles to the EISA/ISA bus, EISA/ISA master read cycles from host memory, DMA read cycles, and during byte assembly or disassembly for EISA masters and DMA cycles addressing EISA/ISA slaves with mismatched data bus sizes.

SYSTEM (EISA/ISA) DATA OUTPUT ENABLE OUTPUT (SD0E0-2#)

These signals enable the output of the data swap buffers/latches onto the EISA/ISA bus. SDOE0# applies to EISA/ISA bus data bits 0-7, SDOE1# to bits 8-15, and SDOE2# to bits 16-31. These signals are enabled during host master write cycles to the EISA/ISA bus, EISA/ISA master read cycles from host memory, DMA read cycles from the host bus, and during byte assembly or disassembly for EISA masters and DMA cycles addressing EISA/ISA slaves with mismatched data bus sizes.

SYSTEM (EISA/ISA) DATA TO HOST DATA LATCH ENABLES OUTPUT (SDHDLE0-3#)

These signals latch the data from the EISA/ISA bus into the data swap latches. The data is then available to be driven onto the host data bus. These signals control the latching of EISA/ISA bus data to host bus data as shown in Table 3-7. The

SDHDSLE# signals are used to latch the data onto the host bus during host read cycles from the EISA/ISA bus, DMA write cycles to host memory, ISA/EISA master write cycles to the host bus, and during byte assembly or disassembly for EISA masters and DMA cycles address EISA/ISA slaves with mismatched data bus sizes.

Table 3-7. EISA/ISA Data to Host Data Latch Operation

Signal	Controls the Latching EISA/ISA BUS Data To Host Bus Data	
SDHDLE0#	Bits (0-7)	Bits (0-7)
SDHDLE1#	Bits (8-15)	Bits (8-15)
SDHDLE2#	Bits (16-23)	Bits (16-23)
SDHDLE3#	Bits (24-31)	Bits (24-31)

HOST DATA OUTPUT ENABLE OUTPUT (HDOE0-1#)

These signals enable the output of the data swap buffers onto the host data bus. HDOE0# applies to host bus data bits 0–15 and HDOE1# applies to bits 16–31. These signals are enabled during host bus master read cycles from EISA/ISA slaves, EISA/ISA master write cycles to the host bus, DMA write cycles to host memory, and during byte assembly or disassembly for EISA masters and DMA cycles addressing EISA/ISA slaves with mismatched data bus sizes.

3.6 Address Buffer Control Signals

NOTE:
There are two address buffer control signals (HALAOE# and LAHAOE#) that function differently depending on the system environment (82350, 82350DT/enhanced, or 82350DT/buffered). The remaining address buffer control signals (HALE#, LASAOE#, LALE#, SALAOE#, and SALE#) function the same, regardless of the system configuration selected.

HOST ADDRESS BUS TO EISA LA BUS OUTPUT ENABLE OUTPUT (HALAOE#)

In 82350 and 82350DT/buffered systems, HALAOE# is active during host bus master, DMA, and refresh cycles. This signal enables the output of the address buffers from the host address bus bits (2–31) to the EISA bus bits (2–31).

In 82350DT/enhanced systems, HALAOE# is active during DMA and refresh cycles only. This signal enables the output of the address buffers from the ISP address bits (2–31) to the EISA LA bus bits (2–31).

HOST ADDRESS LATCH ENABLE OUTPUT (HALE#)

In 82350 and 82350DT/buffered systems, this signal enables the latching of the LA address bus onto the host bus. For EISA and ISA bus masters, HALE# is always held active low to allow the LA bus to propagate to the host.

In 82350DT/enhanced systems, this signal enables the latching of the LA address onto the 82357 (ISP) address bus. For EISA and ISA bus masters. HALE# is always held active low to allow the LA bus to propagate to the ISP.

EISA LA TO EISA SA OUTPUT ENABLE OUTPUT (LASAOE#)

This signal enables the output of the address buffers from the EISA LA bus bits (2–19) to the EISA SA Bus bits (2–19). It is active during host bus master, EISA bus master, DMA, and refresh cycles.

EISA LA TO HOST ADDRESS OUTPUT ENABLE OUTPUT (LAHAOE#)

In 82350, and 82350DT/buffered systems, LAHAOE# enables the output of the address buffers from the EISA LA bus to the host HA bus. It is active during EISA and ISA bus master cycles.

In 82350DT/enhanced systems, LAHAOE# enables the output of the address buffers from the EISA LA bus to the ISP address bus. It is active during EISA, ISA, and host bus master cycles.

LA LATCH ENABLE OUTPUT (LALE#)

This signal controls the latching of the host address bus onto the LA address bus. At its trailing (rising) edge, the latch closes and the LA addresses are held. This signal is used to latch the HA address during host master cycles to the EISA/ISA bus. In an 82350DT/enhanced system, this signal is tied to the 82359 DRAM controller.

EISA SA TO EISA LA OUTPUT ENABLE OUTPUT (SALAOE#)

This signal enables the output of the address buffers from the EISA SA bus bits (2–16) to the EISA LA bus bits (2–16). It is asserted during ISA bus master cycles.

SA LATCH OUTPUT (SALE#)

This signal controls the latching of the LA address bus (bits 2–19) to the SA address bus (bits 2–19).

At the trailing (rising) edge of SALE# the LA address is latched and held until SALE# is driven active. During EISA master cycles, host master cycles, DMA burst back-off cycles, DMA page break cycles, and subsequent assembly/disassembly DMA cycles, SALE# is active while BCLK is low and START# is low. During regular DMA cycles (i.e., no assembly/disassembly required), the initial cycle of an assembly/disassembly DMA cycle, and DMA burst cycles, SALE# is driven active on the rising edge of BCLK that ST0 - ST3 are sampled, and driven inactive at the trailing edge of START#. During ISA master cycles, SALE# is asserted when EMSTR16# is asserted and will remain active until EMSTR16# is driven inactive.

3.7 Reset Control Signals

SYNCHRONOUS POWER OK INPUT (SPWROK)

The synchronous power (ok) signal from the power supply, when driven high, is used to indicate to the 82358DT that the system board has been at the correct voltage long enough for proper operation. In a 386 system environment, the SPWROK signal is synchronized externally to a master 1x clock phase and then used by the 82358DT to synchronize its internal 1x clock (EBC__CLK1). In an i486 system environment, externally synchronizing SPWROK is not necessary. In this case, the 82358DT uses HCLKCPU to synchronize EBC__CLK1.

SYSTEM RESET OUTPUT (RST)

RST is active at power-up and is driven inactive 90 BCLK's (approximately 10 microseconds) after SPWROK is driven active and BCLK is stable. The trailing edge of RST is synchronous to the 82358DT's internal 1x clock (EBC__CLK1). RST, RSTCPU and RST385 are all driven inactive at the same time after power-up.

RESTART INPUT (RSTAR#)

This active low input is the reset signal from the keyboard controller and is used to reset the system under program control. The 82358DT uses it to generate RSTCPU and RST385. The minimum pulse width of RSTAR# is 4 HCLKCPU's. This signal is latched by the 82358DT.

RESET FOR CPU OUTPUT (RSTCPU)

This signal is driven active when a shutdown is decoded or RSTAR# is driven active. This signal comes in active at power-up. RSTCPU is synchronous to the 82358DT's internal 1x clock (EBC__CLK1), and remains active as long as RST (90 BCLKs) or RSTAR# (minimum pulse width 68 HCLKCPU's) remain active. RSTCPU is interlocked with HHOLD so that only one of them is active at a time. If a reset condition other than SPWROK occurs while HHOLD is active, RSTCPU will not be activated until HHOLD is driven inactive. External re-timing of this signal is necessary to meet the setup and hold requirements of the 80386 CPU RESET input.

RESET FOR THE 82385 OUTPUT (RST385)

This signal is driven active under the same conditions that RSTCPU is driven active. After power-up, RST385 is driven inactive with RSTCPU. During a shutdown cycle, or a keyboard controller reset (RSTAR# driven active), RST385 is driven active 16 HCLKCPU's after RSTCPU is driven active and driven inactive concurrently with RSTCPU. The active edge of RST385 is staggered from the active edge of RSTCPU to insure that the 82385 cache controller is not reset in the middle of a CPU cycle to the 82385. External re-timing of this signal is necessary to meet the setup and hold requirements of the 82385 RESET inputs.

3.8 Configuration Signals

CPU TYPE AND FREQUENCY INDICATION INPUT CPU(3–0)

These pins indicate the type of CPU and its frequency on the host bus. CPU3 indicates the CPU data bus width, CPU2 indicates whether HCLKCPU is a 1x or 2x clock and CPU[1:0], along with CPU2 indicate the frequency of HCLKCPU.

Table 3-8. CPU Type/Frequency Indication

CPU[3:0]
1010 - 32-bits, 2x, 25 MHz (25 MHz 80386)
1011 - 32-bits, 2x, 33 MHz (33 MHz 80386)
1100 - 32-bits, 1x, 25 MHz (25 MHz 80486)
1101 - 32-bits, 1x, 33 MHz (33 MHz 80486)

NOTE:
All other bit combinations are reserved.

Bit Definition for CPU[3:0]:

Bit	1	0	
	0	0	25 MHz 486
	0	1	33 MHz 486
	1	0	25 MHz 386
	1	1	33 MHz 386

Bit 2 - 1x or 2x mode

Bit 3 - Reserved (Must be 1)

READY DELAY ENABLE INPUT (RDE#)

This signal is strapped low in systems which require an extra CPU CLK1 delay before HERDYO# and HRDYO# (82350 systems) are asserted or ARDY (82350DT systems) is negated in response to a CPU to EISA/ISA bus read cycle. This allows more time for the data to propagate to the host bus. RDE# is pulled high if the delay is not required.

3.9 Miscellaneous Signals

KEYBOARD CONTROLLER CLOCK OUTPUT (CLKKB)

This signal is used by the keyboard processor and has a nominal duty cycle of 50%. It is generated by dividing HCLKCPU appropriately. Its frequency depends on the CPU[3:0] pins as shown in Table 3-9. CLKKB will begin oscillating after SPWROK is driven high.

Table 3-9. CLKKB Generation

CPU[3:0]	CLKKB Freq	HCLKCPU Divided by
1010 - 25 MHz 80386	10.00 MHz	/5
1011 - 33 MHz 80386	11.00 MHz	/6
1100 - 25 MHz 80486	8.33 MHz	/3
1101 - 33 MHz 80486	11.00 MHz	/3

NOTE:
All other bit combinations are reserved.

LONG WAIT BETWEEN I/O CYCLES INPUT (LIOWAIT#)

This signal controls the delay between back to back 8- and 16-bit ISA I/O slave cycles originating on the host bus. LIOWAIT# is sampled on the trailing edge of the I/O command strobe. If LIOWAIT# is sampled active, the START# signal for the current cycle is delayed until LIOWAIT# is sampled inactive. Once LIOWAIT# is sampled inactive the next cycle can begin. This guarantees a minimum of one added BCLK for I/O recovery time when LIOWAIT# is sampled inactive. The maximum delay is defined by LIOWAIT# being sampled active; three BCLKS for 16-bit I/O slaves, or eleven BCLKS for 8-bit I/O slaves. Delays in between the minimum and maximum are controlled by LIOWAIT# going inactive. No delays are inserted for EISA bus master cycles, CPU cycles to EISA slaves, DMA cycles, or I/O assembly/disassembly cycles. EISA master cycles to ISA I/O slaves need I/O recovery time of 1 BCLK provided by software. Refer to section 4.10 for additional information.

AEN LATCH ENABLE OUTPUT (AENLE#)

AENLE# is used to control the latching of the slot specific AENx (x = slot number) signals. The AENx signals are used by slave devices to determine if they can respond to addresses and I/O commands on the bus. The AENx signals are generated by external logic and are latched on the rising edge of AENLE# and remain latched until AENLE# is driven active. Refer to section 4-15 for a detailed discussion on 82358DT slot support.

BUS CLOCK INPUT (BCLKIN)

This pin is the source of BCLK from which all 82358DT BCLK related timings are triggered. References, diagrams, and specifications that use the generic term ''BCLK'' all refer to the signal supplied to the BCLKIN input. The waveform on BCLKIN must replicate BCLKOUT (i.e., direct connect of BCLKOUT to BCLKIN, or through a non-inverting buffer).

TEST1# INPUT

This active low signal tri-states all outputs of the 82358DT, except BCLK. Under normal system operation, this input should be pulled high with a 10K pullup.

4.0 BASIC FUNCTIONALITY

4.1 82358DT Mode Select and Enhanced Features

The 82358DT provides five mode/function select pins which allow it to be configured for use in either 82350 or 82350DT based systems. The mode pins also provide support for posted memory write cycles to the EISA/ISA bus and 82350DT/i486 burst support. The five mode/function select pins are shown in Table 4-1. The 82358DT will default to 82350 mode without the addition of external logic.

Table 4-1. Mode Description

Signal	Pin #	Description	Note
HNA#/SBMODE#	106	0 - 82350DT host interface 1 - 82350 host interface	4 1, 5
PWEN#	123	0 - Posted memory writes enabled 1 - Posted memory writes disabled	4, 5 2, 4, 5
AMODE	124	0 - 82350, 82350DT/Buffered addr/status buffer control 1 - 82350DT/Enhanced addr/status buffer control	3, 4, 5 4

NOTES:
1. **Default:** internal pullup resistors have been provided to insure these signals default to standard 82350 mode.
2. **Default:** assumes PWEN# Pin 123 is tied high, as indicated in the 82358 (EBC) data sheet.
3. **Default:** assumes AMODE# Pin 124 is tied low, as indicated in the 82358 (EBC) data sheet.
4. 82350DT chip set compatible.
5. 82350 chip set compatible.

The functions associated with the mode/function select signals HNA#/SBMODE and HBE[1:0]# are selected by driving them either high or low on the rising edge of SPWROK (refer to Figures 8-12 and 8-15). The posting of memory writes can be enabled by tying PWEN# low with a 1K pulldown resistor or disabled by tying PWEN# high with a 10K pullup resistor. PWEN# can also be changed dynamically, in which case it must meet the setup and hold times as indicated by specs t63 through t63c. The function associated with AMODE can be selected by either tying it high with a 10K pullup or low with a 1K pull-down, depending on the function desired.

4.1.1 HOST BUS INTERFACE MODE SELECT (*HNA#/SBMODE#*)

The host bus interface unit interfaces to either the host bus protocol of the 386 or i486 microprocessors (82350 environment) or the system bus protocol of the 82359 DRAM controller (82350DT environment), depending on the sampling of HNA#/SBMODE# at power-up. If HNA#/SBMODE# = 1, the 82358DT is selected to operate in an 82350 system environment. If the HNA#/SBMODE# = 0, the 82358DT is selected to operate in an 82350DT system environment. Figures 2-5 through 2-7 illustrate these basic host interfaces.

There are four host multiplexed cycle control signals that change in function depending on the mode selected. These signals are shown in Table 4-2. The remaining host signals functionally remain the same, regardless of the mode selected. A detailed description of the multiplexed control signals can be found in the pin description section, section 3.1.1.

Table 4-2. Multiplexed Host Bus Control Signals

Pin #	82350 Compatible (SBMODE# = 1)	82350DT Compatible (SBMODE# = 0)
72	HADS0#	AS#
114	HERDYO#	ARDY
112	HRDYO#	SDVLD
127	HRDYI#	1 KΩ Pull-Up

4.1.2 ADDRESS/STATUS BUFFER CONTROL MODE (*AMODE*)

4.1.2.1 Enhanced and Buffered Configurations

In an 82350DT system environment, there are two techniques used to interface the CPU address and control signals (M-IO and W-R) to the EISA bus. The first and most common method, referred to as the enhanced configuration (AMODE = 1), requires that the address bus from the 82357 DMA controller (ISP) be buffered separately from the address bus, M-IO, and W-R control signals generated by the 82359 DRAM controller. In this configuration, the address, M-IO, and W-R signals from the 82359 are driven directly to the EISA bus, while the address and W-R signals from the ISP are buffered through

the EBB (refer to Figure 4- 2). The second method, referred to as the buffered configuration (AMODE = 0), requires that the address bus from the ISP be buffered together with the address bus, M-IO, and W-R control signals generated by the 82359 (refer to Figure 4-3).

The enhanced method is preferred in an 82350DT chip set design to insure that EISA bus specifications are met. The buffered method is targeted for advanced 82350DT systems which require additional I/O peripherals on the motherboard. These additional I/O devices would reside on the buffered bus (refer to Figure 2-3).

In an 82350 system environment, the buffered configuration (AMODE = 0) is used. The buffered configuration is 82358 EBC(Ax) compatible (refer to Figure 4-1).

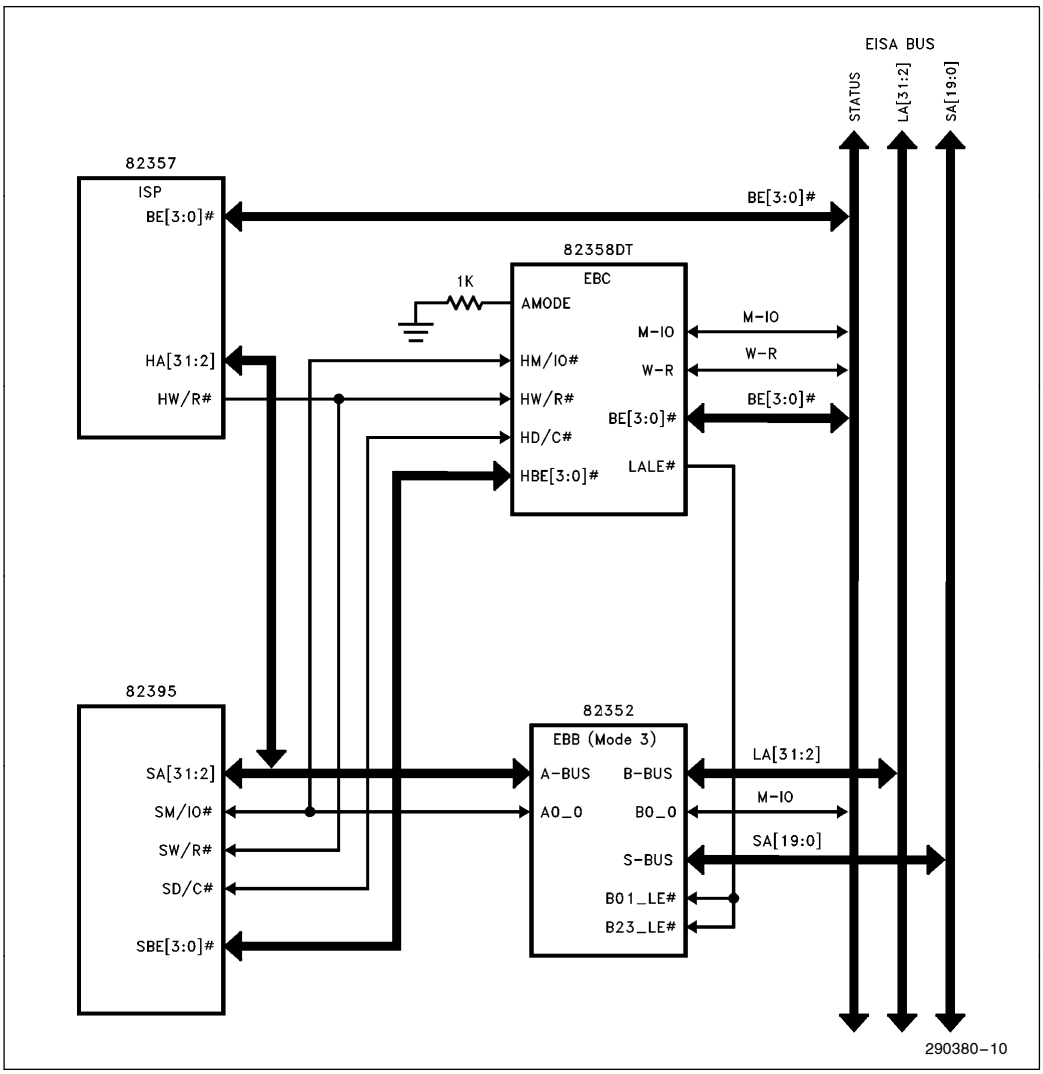


Figure 4-1. 82350 Configuration

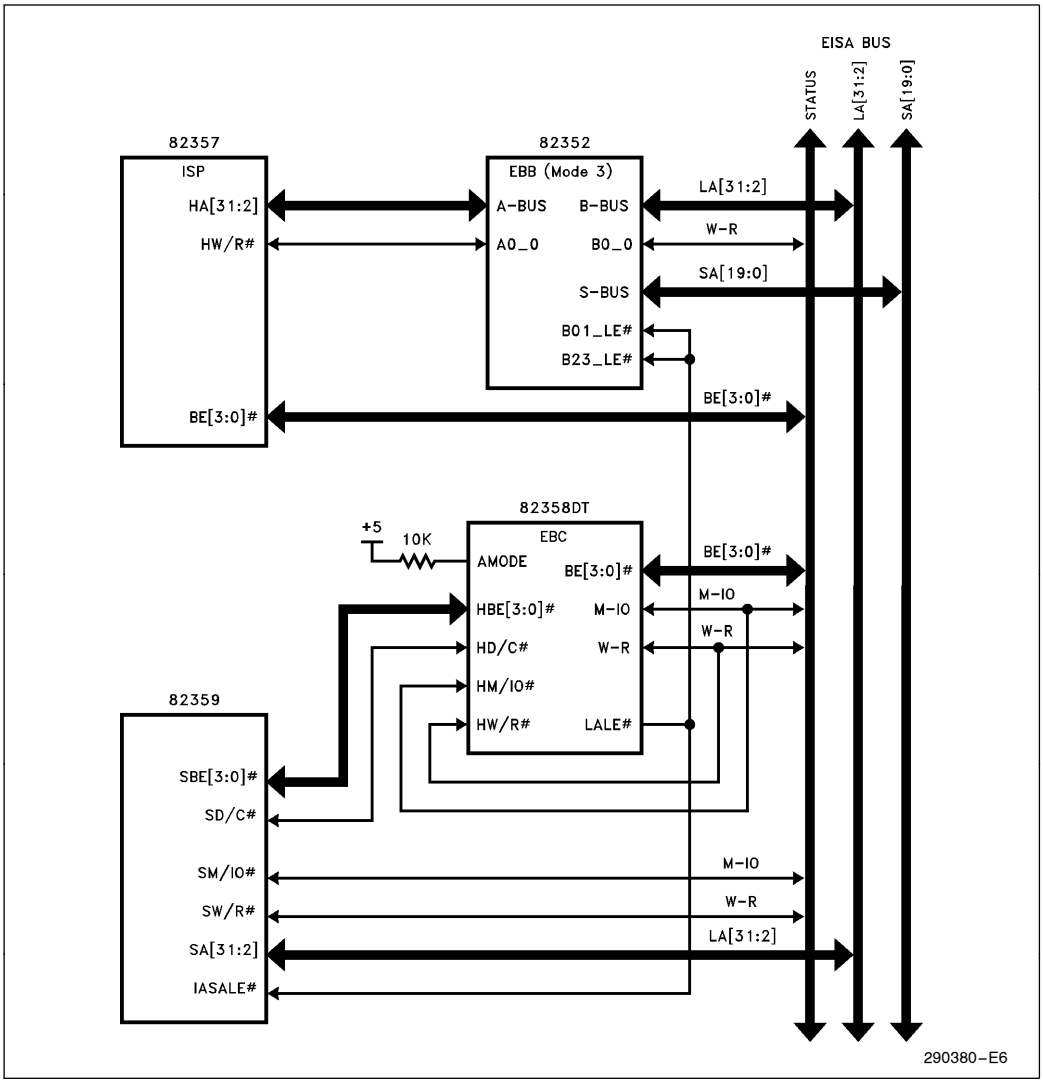


Figure 4-2. 82350DT/Enhanced Configuration

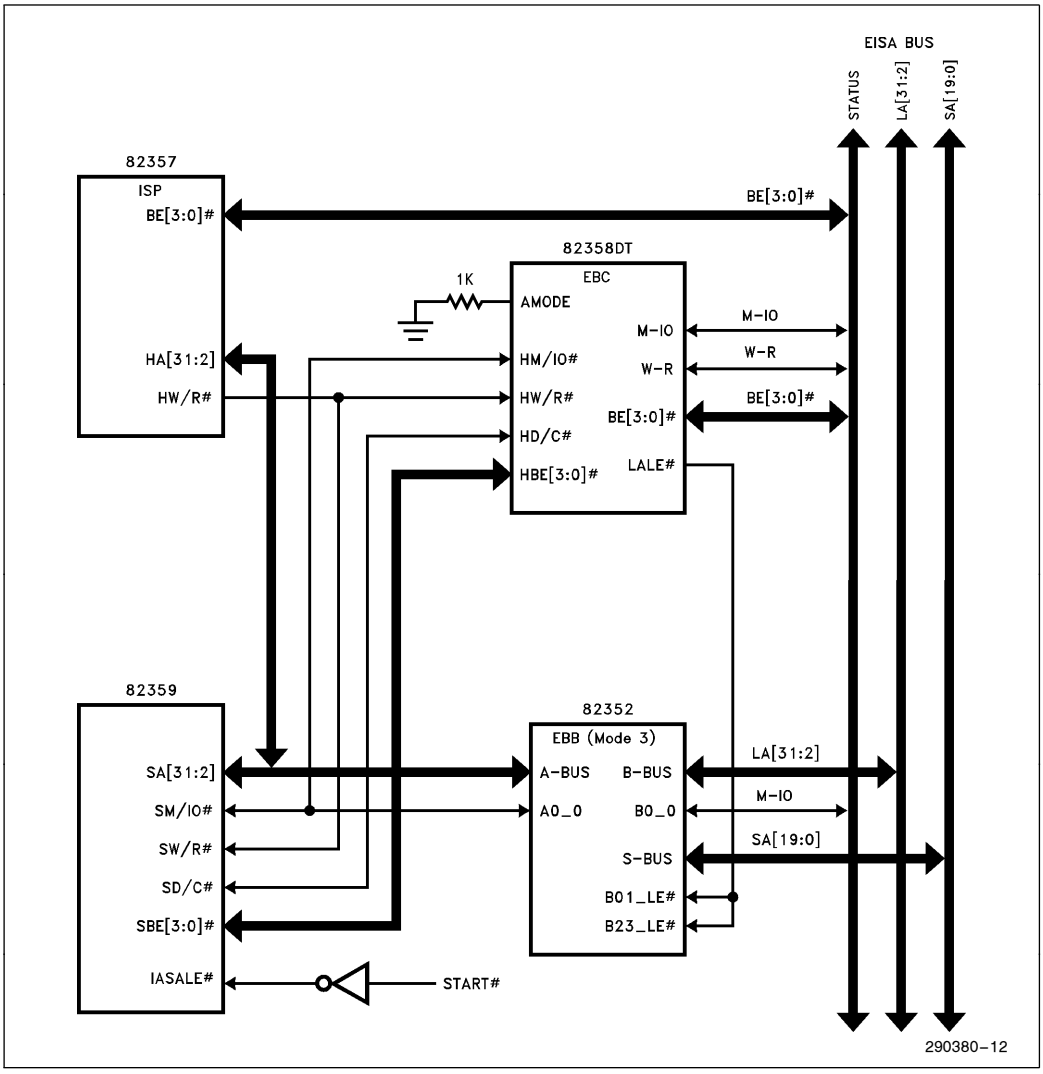


Figure 4-3. 82350DT/Buffered Configuration

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4.1.2.2 Host Status Control (M-IO and W-R)

As discussed earlier, in an 82350DT/enhanced configuration, the 82359 DRAM controller drives the EISA bus signals M-IO and W-R directly, bypassing the 82358DT and EBB devices. To prevent contention between the 82358DT host status signals (HM/IO# and HW/R#) and the respective EISA status signals (M-IO and W-R), the 82358DT will float the host or EISA status signals as required, depending on the current bus master (refer to Table 4-15, section 4.8).

4.1.2.3 Address Buffer Control

In an 82350DT/enhanced configuration (AMODE = 1), the address generated by the 82359 DRAM controller on behalf of the host CPU, drives the EISA bus directly. As a result, the function of the HALAOE# and LAHAOE# address buffer output enable signals function differently, depending on the mode selected. This is shown in Tables 4-3 and 4-4. Table 4-3 shows the function of HALAOE# and LAHAOE# when used in an 82350DT/enhanced configuration (AMODE = 1). Table 4-4 shows the function of HALAOE# and LAHAOE# when used in either an 82350 or 82350DT/buffered configuration (AMODE = 0).

Table 4-3. Enhanced Implementation (AMODE = 1)

Signal	Active during the Following Cycles
HALAOE#	DMA and Refresh Cycles
LAHAOE#	HOST Master, EISA Master, and ISA Master Cycles

Table 4-4. Buffered Implementation (AMODE = 0)

Signal	Active during the Following Cycles
HALAOE#	HOST Master, DMA, and Refresh Cycles
LAHAOE#	EISA Master, and ISA Master Cycles

The remaining buffer control signals, LASAOE#, SALAOE#, HALE#, LALE#, and SALE#, function the same, regardless of the mode selected.

4.1.3 POSTED WRITES (*PWEN#*)

To optimize the performance of memory write cycles, the 82358DT will dynamically post write cycles to the EISA/ISA bus. The host portion of the cycle is terminated on the host bus by activating the rising edge of ARDY (82350DT designs) or the falling edge of HERDY0# (82350 designs) after the latching of host write data by the 82353 (82350DT design) and the 82352 (82350 design) data buffers. The write data is latched on the rising edge of HDSDLE1# during START# active. Posting of memory writes is only performed if PWEN# is sampled active on the rising edge of HCLKCPU at the start of the cycle that requires posting. The 82358DT will only post host memory write cycles to the EISA or ISA bus. The dynamic nature of PWEN# allows posting of specific cycles to be disabled (e.g., memory mapped I/O cycles). If PWEN# is sampled inactive at the start of a memory cycle, that cycle will not be posted. PWEN# can also be tied low if differentiating between which memory write cycles can and can not be posted is not necessary. Figures 5-10, 5-11, and 5-14 through 5-16 in the basic function timing section, section 5.0, show the posting of memory write cycles in both an 82350 and an 82350DT system.

During back-to-back posted write cycles, the termination of the second posted write will not occur until one BCLK after CMD# is driven inactive for the first posted write cycle. This insures that the DATA hold time of the first posted write cycle is not violated. Also during the second cycle of back-to-back posted write cycles, HDSDLE1# is driven active on the falling edge of BCLK during START#, and then inactive on the rising edge of HCLKCPU at the end of START#.

If a posted write cycle is in progress, and the 82357 (ISP) arbiter requests the bus via DHOLD, the 82358DT will not drive HHOLD active to the CPU until the actual EISA/ISA write cycle is complete (even though ARDY or HERDYO# are returned earlier). This prevents the ISP from giving the bus to another master before the 82358DT has completed the posted write cycle on the EISA/ISA bus. If after this point, HHLDA is not returned active and another memory write cycle is initiated, the 82358DT will *not* post the write or any future writes (i.e. the initiated cycle and all future cycles will be run as a non-posted write) until DHOLD from the ISP has been returned low again.

4.2 EISA/ISA Bus Cycle Types and Duration

Table 4-5 below shows the type of cycles the 82358DT runs on the EISA/ISA bus. Table 4-6 shows the number of BCLKS that occur for each cycle type.

Table 4-5. Types of Cycles 82358DT Runs on EISA/ISA Bus

DMA	ISA & EISA	EISA Only
Type A	Default (Standard) memory	Burst
Type B	Default (Standard) I/O	
Type C (Burst)	NOWS# memory	
Compatible	NOWS# I/O	

In Table 4-6, No Wait States refers to a standard cycle that has been shortened by an ISA slave driving NOWS# active at the beginning of the transfer (note: NOWS# can dynamically shorten the cycle by one, two, or three BCLKs). Standard cycle refers to an ISA cycle that has not been shorten with NOWS# or extended with CHRDY, or an EISA cycle that has not been extended with EXRDY. One wait state applies when CHRDY or EXRDY is used to extend the standard cycle by one BCLK. As an example, an ISA 8-bit standard memory read cycle will run cycles lasting six BCLKs, or if NOWS# is sampled active, it will run a no wait state cycle lasting three, four, or five BCLKs, depending on when NOWS# is driven active. As a note, if CHRDY and NOWS# are active during the same cycle, CHRDY will override NOWS#, and wait states will be added to the standard cycle.

Table 4-6. EISA/ISA/DMA Bus Cycles

Number of BCLKs per Cycle						
Slave Operation	**Bus Size (In Bits)**	**No Wait State**	**One Standard Cycle**	**Wait State**	**Burst Cycle**	**Max. Transfer Rate At 8.33 MHz**
EISA Cycles(1)						
MEMORY READ	32/16	NA	2	3	1	33.33 Mb/sec(6)
MEMORY WRITE	32/16	NA	2	3	1	33.33 Mb/sec(6)
I/O READ	32/16	NA	2	3	NA	16.66 Mb/sec(6)
I/O WRITE	32/16	NA	2	3	NA	16.66 Mb/sec(6)
ISA Cycles(1)						
MEMORY READ	16	2	3	4	NA	8.33 Mb/sec
MEMORY READ	8	3,4,5	6	7	NA	2.78 Mb/sec
MEMORY WRITE	16	2	3	4	NA	8.33 Mb/sec
MEMORY WRITE	8	3,4,5	6	7	NA	2.78 Mb/sec
I/O READ	16	3	3	4	NA	5.56 Mb/sec
I/O READ	8	3,4,5	6	7	NA	2.78 Mb/sec
I/O WRITE	16	3	3	4	NA	5.56 Mb/sec
I/O WRITE	8	3,4,5	6	7	NA	2.78 Mb/sec
INTA READ	NA	NA	6	NA	NA	NA
DMA Cycles(2,3,4,5)						
COMPATIBLE	ALL	8	8	10	NA	4.17 Mb/sec(6)
TYPE A	ALL	6	6	7	NA	5.56 Mb/sec(6)
TYPE B	ALL	4	4	5	NA	8.33 Mb/sec(6)
TYPE C (BURST)	32/16	3	3	4	1	33.33 Mb/sec(6)

NOTES:
1. The EISA and ISA slave cycles are measured from the falling edge of START# to the rising edge of CMD#.
2. The DMA cycles are measured from the BCLK edge that the LA address is valid to the BCLK edge that CMD# is driven inactive.
3. DMA I/O devices can not add wait states.
4. During DMA compatible cycles when CHRDY is sampled active, one wait state of two BCLK duration is added. When EXRDY is sampled active, a wait state of one BCLK duration is added.
5. NOWS# driven active during DMA cycles has no effect on the cycle, except during the subsequent cycles of an assembly or disassembly transfer, and only if the memory device is ISA. The cycles are shortened as indicated for ISA memory slaves.
6. Assumes 32-bit bus size.

4.3 82358DT Cycle Translation

The 82358DT automatically translates and broadcasts cycles between the host, EISA, and ISA buses, as required.

Tables 4-7 and 4-8 illustrate how the 82358DT determines the type of master and slave involved in the transfer. Table 4-9 illustrates the type of cycle or cycles broadcasted, depending on the master/slave combination.

82358DT CYCLE TRANSLATION AND BROADCASTING ALGORITHM

A. The 82358DT determines the master type and size (Host/EISA/ISA/DMA) as shown in Table 4-7.

B. The 82358DT determines the slave type and size (Host/EISA/ISA/DMA) as shown in Table 4-8.

C. The 82358DT broadcasts the required cycle types depending on the master and slave combination (refer to Table 4-9). Assembly/disassembly cycles are run according to the master/slave size combination.

Table 4-7. 82358DT Determines Bus Master Type

HHLDA	REFRESH#	EXMASTER#	MASTER16#	EMSTR16#	MSBURST#	SIZE	MASTER
0	1	1	1	1	1	32	HOST(1)
1	0	1	1	X	1	ALL	REFRESH
1	1	0	1	1	1	32	EISA
1	1	0	1	1	0	32	EISA (Burst)
1	1	0	1-0 (pulse)	1	0	16	EISA (Burst)(2)
1	1	0	0	1	1	16	EISA
1	1	0	0	1	0	16	EISA (Burst)
1	1	1	0	0	1	16	ISA
1	1	1	1	1	1	ALL	DMA
1	1	1	1	1	0	ALL	DMA (Burst)

NOTES:
1. It is the systems designers responsibility to insure that a master located on the buffered bus (82358DT strapped for an 82358DT/buffered configuration) is part of the system bus arbitration scheme. The above condition assumes that the buffered master is gaining access to the bus through the ISP's CPUMISS# input.
2. This applies to a downshifting master. When downshifting from a 32- to 16-bit EISA burst bus master, the bus master must drive MASTER16# active during START# for each cycle that it generates.

Table 4-8. 82358DT Determines Slave Type

HLOCMEM#	HLOCIO#	EX32#	EX16#	M16#	IO16#	Size	Slave
0	X	(1), (3)	1	X	X	32	HOST MEMORY
X	0	(1), (3)	1	X	X(1)	32	HOST I/O
1	1	0	X	X	X	32	EISA
1	1	1	0	X	X	16	EISA
1	1	1	1	0	X	16	ISA MEMORY
1	1	1	1	X	0	16	ISA I/O
1	1	1	1	1	X	8	ISA MEMORY
1	1	1	1	X	1	8	ISA/EISA I/O(2)

NOTES:
X = Signal not decoded.
1. During EISA master accesses to Host slaves, the 82358DT drives EX32# active. During ISA master accesses to Host slaves, the 82358DT drives IO16# active if HLOCIO# is active.
2. The 82358DT will not generate EISA cycles during ISA master to 8-bit EISA memory slaves.
3. If EX32# is driven active during an ISA master cycle to a host slave, the 82358DT will generate an EISA cycle and reference the data swap control signals to START# and CMD#.
4. When determining slave type, the 82358DT also uses MIO#, HMIO#, IOWC# or IORC#, depending on the master type (Host, EISA, ISA), to qualify the slave decode signals in Table 4-8.

Table 4-9. 82358DT Determines Which Cycles to Broadcast

MASTER/SLAVE COMBINATION		
MASTER	**SLAVE**	**CYCLE BROADCASTED BY 82358DT**
HOST	HOST	NO EISA or ISA CYCLE BROADCASTED
HOST	EISA	EISA CYCLE BROADCASTED
HOST	ISA	ISA and EISA CYCLES BROADCASTED
EISA	HOST	NO HOST or ISA CYCLE BROADCASTED
EISA	EISA	NO ISA CYCLE BROADCASTED
EISA	ISA	ISA CYCLE BROADCASTED
ISA	HOST	NO HOST CYCLE BROADCASTED, EISA CYCLE BROADCASTED IF HOST DRIVES EX32# ACTIVE
ISA	EISA	EISA CYCLE BROADCASTED
ISA	ISA	EISA CYCLE BROADCASTED, EXCEPT ISA MASTER TO ISA MEMORY SLAVE
DMA	ALL	EISA AND ISA CYCLES BROADCASTED

NOTES:
1. In the above table:
EISA CYCLE BROADCASTED = BALE#, SA[1:0], SBHE#, BE[3:0]#, M-IO, W-R, LOCK# START, and CMD#.
ISA CYCLE BROADCASTED = BALE#, SA[1:0], SBHE#, IORC#, IOWC#, MRDC#, MWTC#, SMRDC#, SMWTC#.
2. During a HALT or SHUTDOWN cycle, EISA and ISA cycles are not broadcasted.

4.4 Data Size Translation (Data Buffer/Latch Swap Logic)

4.4.1 DATA BUFFER/LATCH SWAP LOGIC

The data swap logic provides the assembly/disassembly, copy up/copy down, re-drive, and latching functions between the host and EISA/ISA buses. A discrete representation of the data swap logic is shown in Figure 4-4. A summary of the data swap logic operations is shown in Table 4-10.

In an 82350, and an 82350DT/buffered environment, the data swap logic is implemented using an EISA Bus Buffer (EBB) selected for data mode (mode 0). The data swap logic is placed between the EISA/ISA bus and the host bus as shown in Figures 4-5 and 4-6.

In an 82350DT/enhanced environment, the data swap logic is implemented using two 82353 (ADP) devices. The swap logic is positioned in this system as shown in Figure 4-7.

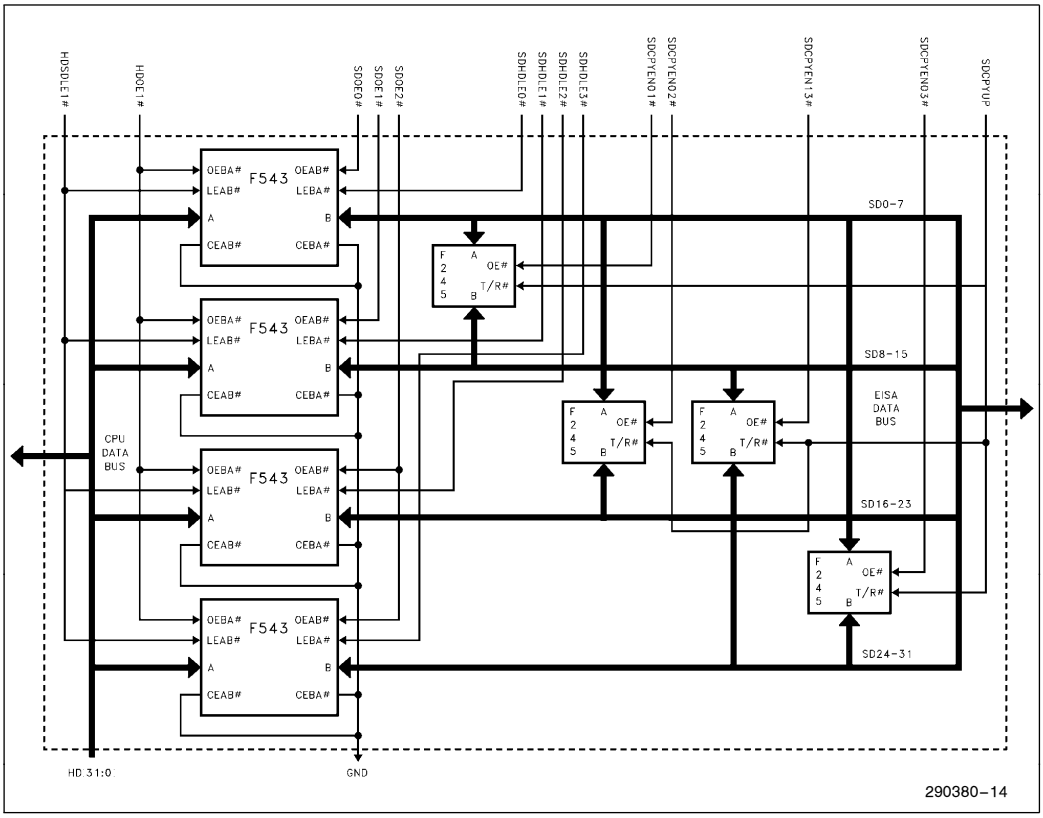

Figure 4-4. Discrete Representation of Data Swap Logic

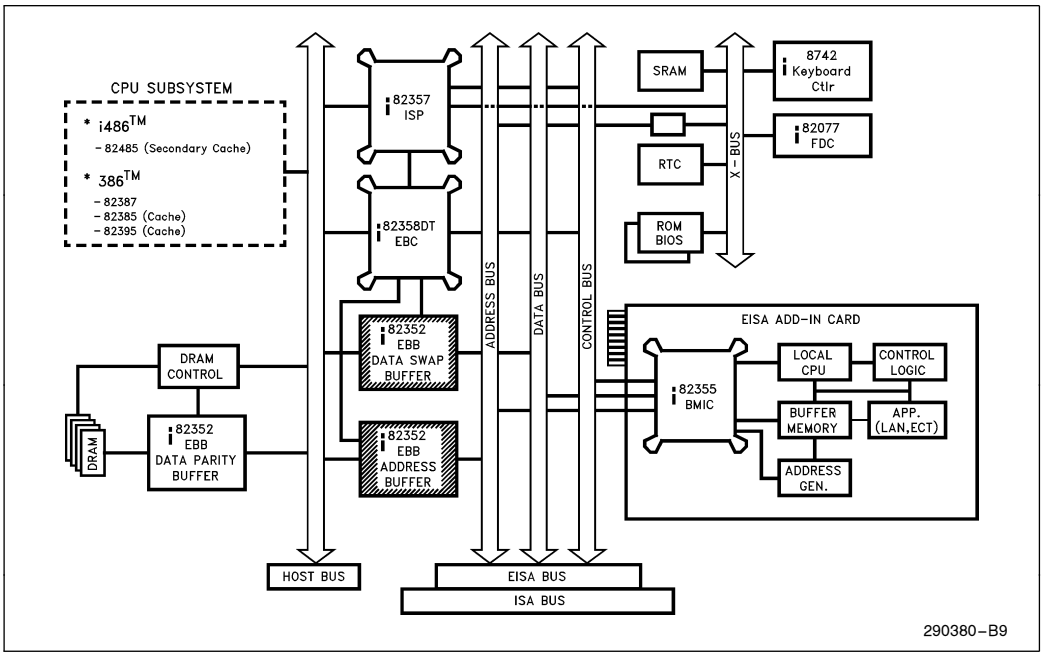

Figure 4-5. Data Swap Logic (82350 System)

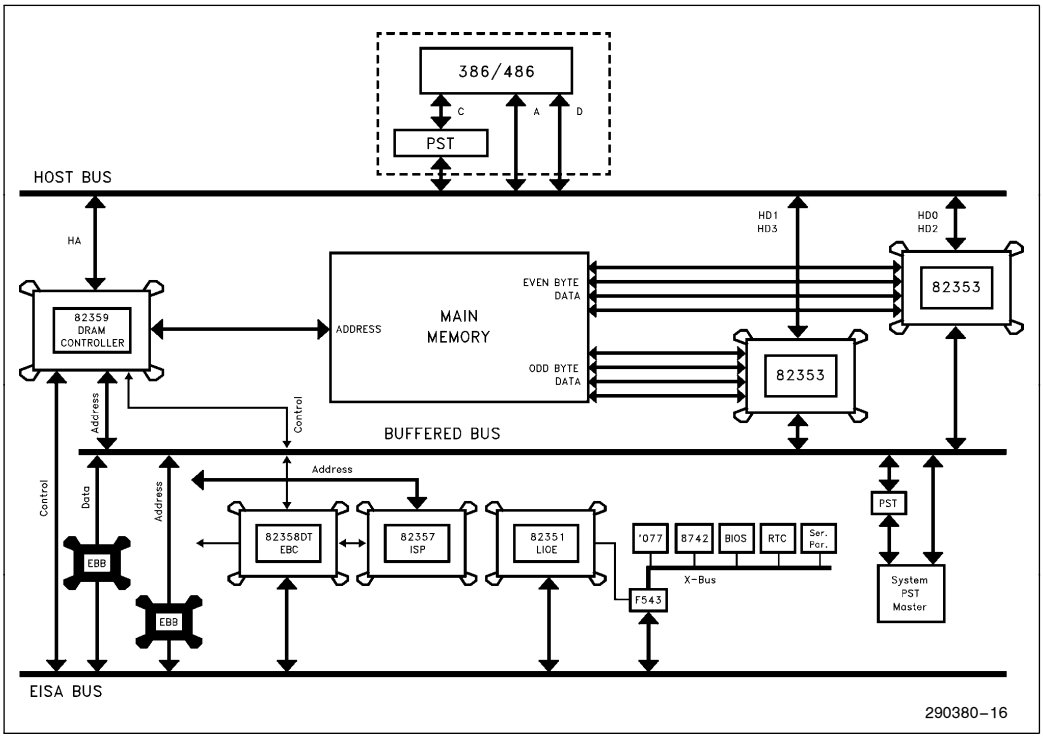

Figure 4-6. Data Swap Logic (82350DT System/Buffered Configuration)

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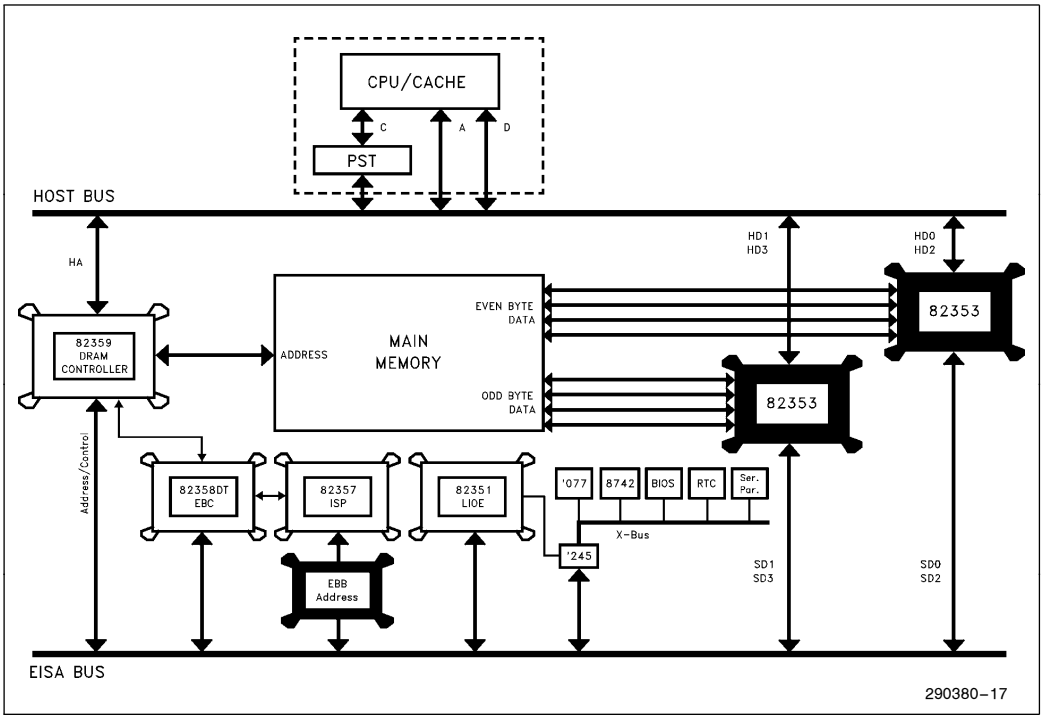


Figure 4-7. Data Swap Logic (82350DT System/Enhanced Configuration)

4.4.2 DATA SIZE TRANSLATION

Data size translation is performed by the 82358DT when the master (in the case of a DMA cycle, this would be the I/O device) and slave data bus sizes do not match (e.g., 32-bit EISA master accessing a 16-bit ISA slave). During a data size translation, the 82358DT will perform one or more of the following operations, depending on the master/slave data size combination, master/slave type (Host/EISA/ISA), transfer direction (read/write), and the number of byte enables active: **data assembly, data disassembly, data copying (up or down), or data redrive.**

The assembly/disassembly process occurs during host, EISA, and DMA cycles where the masters data size is greater than the slaves data size. For example: if a 32-bit host master is performing a 32-bit read cycle to an 8-bit ISA slave, the 82358DT will perform four read cycles to assemble the data (refer to Figure 4-8). The 82358DT will then transfer the data as a single doubleword to the 32-bit host master during the fourth cycle. For a 32-bit write cycle, the 82358DT will dissemble the doubleword by performing four write cycles to the slave. The number of cycles run per transfer is a function of the number of bytes requested (BE[3:0]#) and the master/slave bus size combination. In the case of a DMA transfer, this same example and concept would apply, however, a DMA device (I/O) would be designated as the master device.

During EISA master assembly/disassembly transfers, cycle control is transferred from the master to the 82358DT during the first cycle of the transfer (refer to section 4.5). The master floats its START#, BE[3:0]#, and data lines on the first falling edge of BCLK after START# is negated. At the end of the assembly or disassembly process, cycle control is transferred back to the bus master; indicated by the 82358DT driving EX16# and EX32# active. An additional BCLK is added at the end of the transfer to allow the exchanging of cycle control to occur. During DMA transfers, cycle control is maintained by the 82358DT through-out the entire cycle.

The copy function is enabled during data transfers between byte lanes. For example, in the above host master to 8-bit ISA slave accesses, the data is copied up during the assembly operation and copied down during the disassembly process. The copy-up and copy-down operations are also used during transfers where assembly/disassembly is not required. Specifically, these transfers include EISA master, ISA master, and DMA cycles where the masters data size is smaller than the slaves data size, and transfers between mismatched master/slave combinations where only single bytes or words are transferred. The number of bytes copied-up or copied-down is a function of the number of bytes requested (BE[3:0]#) and the master/slave bus size combination. Figure 4-9 shows a host master reading a signal word from a 16-bit EISA/ISA slave.

During EISA master cycles where data copying is performed, cycle control is transferred from the master to the 82358DT, except during transfers where the masters data size is smaller than the slaves data size (refer to section 4.5). During DMA transfers, cycle control is maintained by the 82358DT through-out the entire cycle.

The re-drive function is enabled when both the master and slave are on the EISA/ISA bus, and the master/slave data size combination is mismatched (e.g., 32-bit EISA master accessing an 8-bit ISA slave). Specifically, re-drive will occur during EISA master and DMA cycles (excluding DMA compatible cycles) where the masters data size is greater than the slaves data size, during EISA master cycles to ISA slaves where the data size of the master and slave are matched, and during DMA burst write cycles to non-burst memory where the DMA devices data size is less than the memory slaves data size.

During a re-drive cycle, the data is latched from the EISA/ISA bus, and then driven back onto the appropriate EISA/ISA byte lanes. During a read cycle, the re-drive occurs after the necessary subcycles have been completed and the read data has been assembled. For example: during a 32-bit EISA master 32-bit read from an 8-bit EISA slave, the data is assembled in four cycles and then re-driven on the fourth cycle (refer to Figure 4-10). During a write cycle, the re-drive occurs after the write data from the master has been latched, and before the data has been disassembled. For example: during a 32-bit EISA master 32-bit write to an 8-bit EISA slave, in the first cycle of the transfer, the 82358DT latches the write data (DWORD) from the master and drives the first byte back onto the lower byte lane of the EISA/ISA bus. The 82358DT will re-drive the second, third, and fourth byte on the second, third, and fourth cycle of the transfer. The number of cycles run per transfer is a function of the BE[3:0]# and the master/slave bus size combination.

During EISA master cycles, the control of the cycle is transferred from the EISA master to the 82358DT before the data is re-driven onto the bus as discussed in section 4.5. During DMA transfers, cycle control is maintained by the 82358DT through-out the entire cycle.

During EISA master and DMA write cycles between master and slave combinations on the EISA/ISA bus, where only copying is required and no assembly or disassembly is necessary (i.e., a one or two byte transfer), the 82358DT will treat this as a re-drive cycle. For example: during a write transfer between a 32-bit EISA master and a 16-bit EISA or ISA slave, where the master is driving data on the upper two byte lanes (BE[3:0]# = 0011), the 82358DT will latch the data on byte lanes 2 and 3. The 82358DT will then re-drive the data onto byte lanes 2 and 3 while copying the data down to byte lanes 0 and 1, for latching by the slave device. This example is shown in Figure 4-11.

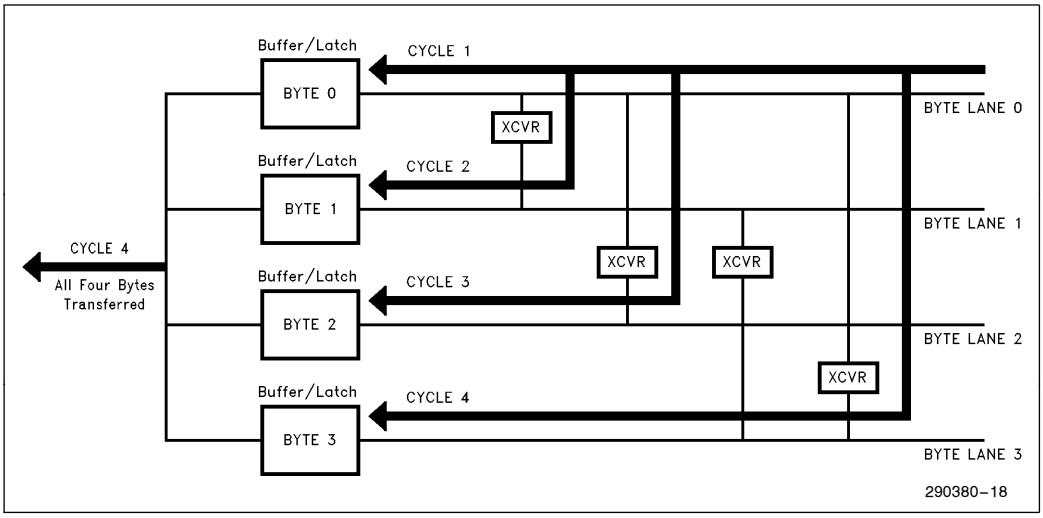


Figure 4-8. Assembly (Host 32-Bit Read from an 8-Bit EISA or ISA Slave — BE[3:0]# = 0000)

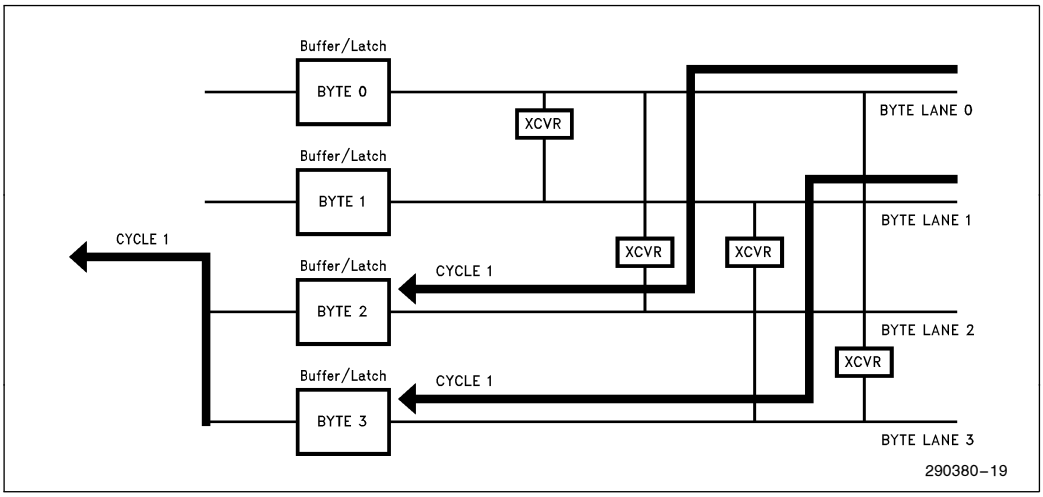


Figure 4-9. Copy Function (Host 16-Bit Read from a 16-Bit EISA or ISA Slave — BE[3:0]# = 0011)

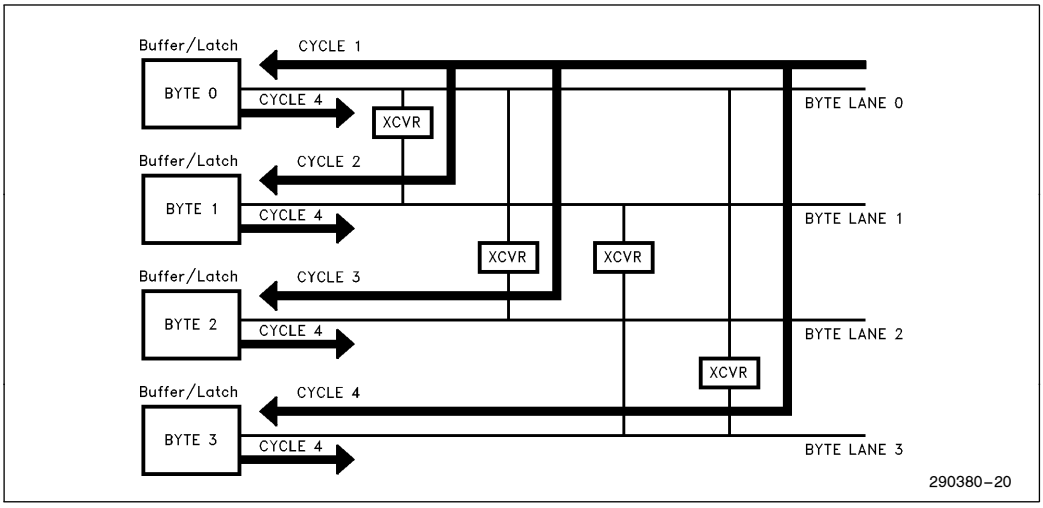


Figure 4-10. Re-Drive Function (32-Bit EISA Master Accessing an 8-Bit EISA or ISA Slave — 32-Bit Read/BE[3:0]# = 0000)

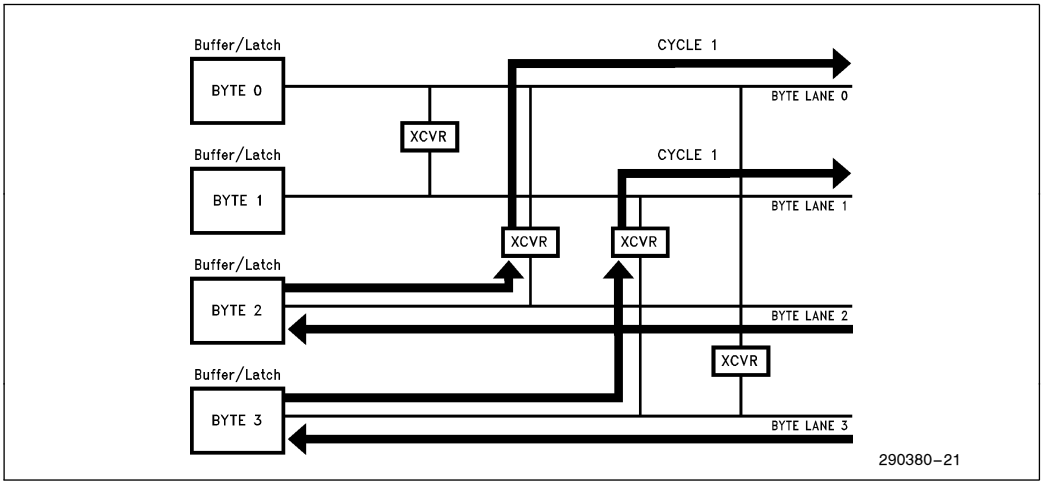


Figure 4-11. Copy with Re-Drive (32-Bit EISA Master Accessing a 16-Bit EISA or ISA Slave — One Word Write/BE[3:0]# = 0011)

The following table summarizes the data size translations (assembly, disassembly, re-drive, and copy functions) for all possible master/slave combinations.

Table 4-10. Data Swap Logic Operation

Master Type/Size or DMA Device Type/Size	Slave Type/Size					
	HOST 32-Bit	EISA 32-Bit	EISA 16-Bit	EISA 8-Bit	ISA 16-Bit	ISA 8-Bit
HOST 32-Bit	S	S	A/D	A/D	A/D	A/D
EISA 32-Bit	S	S	RA/D	RA/D	RA/D	RA/D
EISA 32 to 16-Bit (Downshift)	S	S	S/RA/D	RA/D	RA/D	RA/D
EISA 16-Bit	SCW	SCW	S	RA/D	S	RA/D
ISA 16-Bit	SCW	SCW	S	SC	S	SC
DMA Device 32-Bit	S	S	RA/D	RA/D	RA/D	RA/D
DMA Device 16-Bit	SCW	SCW	S	RA/D	S	RA/D
DMA Device 8-Bit	SCB1	SCB1	SCB1	S	SCB1	S
DMA Device 32-Bit (Compatible)	S	S	SCB2	SCB2	SCB2	SCB2
DMA Device 16-Bit (Compatible)	SCW	SCW	S	SCB2	S	SCB2
DMA Device 8-Bit (Compatible)	SCB1	SCB1	SCB1	S	SCB1	S

NOTES:
S - Single Cycle (no assembly/disassembly or copying).
SC - Single Cycle (no assembly/disassembly, copying between byte lanes 0 and 1 if required). 16-bit ISA masters are required to perform data assembly/disassembly when accessing 8-bit slaves.
SCB1 - Single cycle with copy buffers enabled (SDCPYEN01#, 02#, or 03#), as required by the size of the master and slave, and number of byte enables driven active. The copy direction is determined by the master/slave size combination and read/write indicator.
SCB2 - Single cycle with copy buffers enabled (SDCPYEN01#, 02#, 03#, 13#), as required by the size of the master and slave, and number of byte enables driven active. The copy direction is determined by the master/slave size combination and read/write indicator.
SCW - Single cycle with word copy buffers enabled (SDCPYEN02# and 13#), as required by the size of the master and slave, and number of byte enables driven active. The copy direction is determined by the master/slave size combination and read/write indicator.
A/D - Assembly/disassembly as required by the byte enable combination. No re-driving of the EISA/ISA bus is required. The direction of the data is determined by the master/slave bus location and the read/write indicator. If the transfer can be done in one cycle (i.e., no assembly/disassembly required), the cycle will operate and run as a single cycle.
RA/D - Assembly/disassembly as required by the byte enable combination. Re-driving of the EISA/ISA bus is required. The direction of the data is determined by the master/slave size combination and the read/write indicator.
S/RA/D - A 32-bit downshifting master will downshift to 16 bits and run single cycles only if the 16-bit slave can burst. If the 16-bit slave can not burst, assembly/disassembly cycles will be run.

4.5 EISA Master Back-Off During Mismatched Data Size Transfers

During an EISA master transfer where the master and slave data size is mismatched (refer to Table 4-11), the EISA master is required to back-off the bus on the first falling edge of BCLK after START# is negated. The EISA master floats its START#, BE[3:0]#, and data lines at this time. This allows the 82358DT to perform data size translation, if necessary. The master must back-off the bus if a master/slave data size mismatch is determined, regardless if data size translation is performed.

At the end of the data size translation or transfer, cycle control is transferred back to the bus master; indicated by the 82358DT driving EX16# and EX32# active on the falling edge of BCLK, before the rising edge of BCLK that the last CMD# is negated. An additional BCLK is added at the end of the transfer to allow the exchanging of cycle control to occur.

Figure 4-12 shows a 32-bit EISA master accessing (read or write) a 16-bit EISA slave. The first transfer is a doubleword transfer (multiple cycles required), followed by a single byte request (single cycle required).

Table 4-11. EISA Master Data Size Mismatch

Master Type/Size Cycle Type		Slave Size/Type			
		32-Bit EISA	16-Bit EISA	16-Bit ISA	8- Bit ISA
32-Bit EISA (no downshift capability	Non-Burst Burst	M M	MM,B X	MM,B X	MM,B X
32-Bit EISA (downshift capability)	Non-Burst Burst	M M	MM,B M	MM,B X	MM,B X
16-Bit EISA	Non-Burst Burst	MM MM	M M	MM,B X	MM,B X

M = Matched data size
MM = Mismatched data size
B = Master back-off required
X = Cycle will never occur

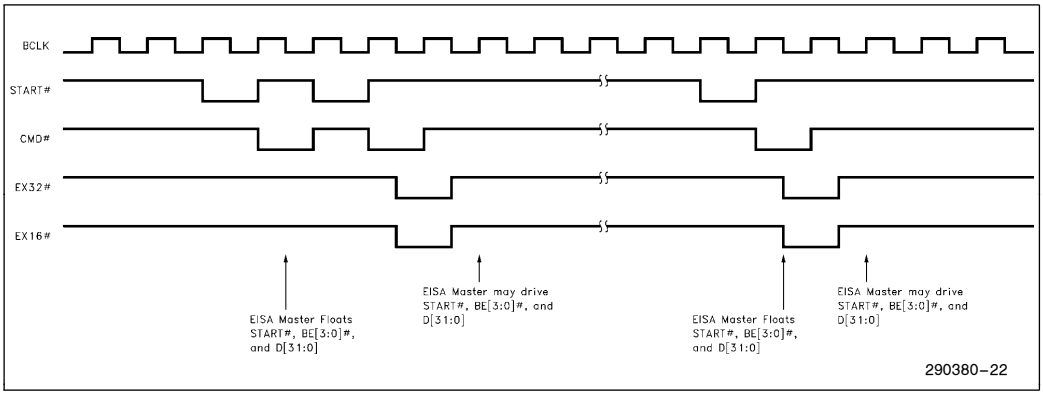


Figure 4-12. EISA Master Back-Off

4.6 Address Translations (Address Buffer/Latch Logic)

The address buffer/latch logic provides the address path between the host and EISA/ISA buses. A discrete representation of the address logic is shown in Figure 4-13. A summary of the drive and latch functions is shown in Table 4-12.

In an 82350, and an 82350DT/buffered system, the address buffers are implemented using an EISA Bus Buffer (EBB) selected for address mode (mode 3). The EBB's are used for address communication between the LA, SA, and host address buses. The EBB is positioned as shown in Figures 4-5 and 4-6.

In an 82350DT/enhanced system, the address buffers are also implemented using an EISA Bus Buffer (EBB). However, in this system the host address lines (82359 SA[31:2]) are connected directly to the LA address bus, bypassing the EBB (refer to Figure 4-2).

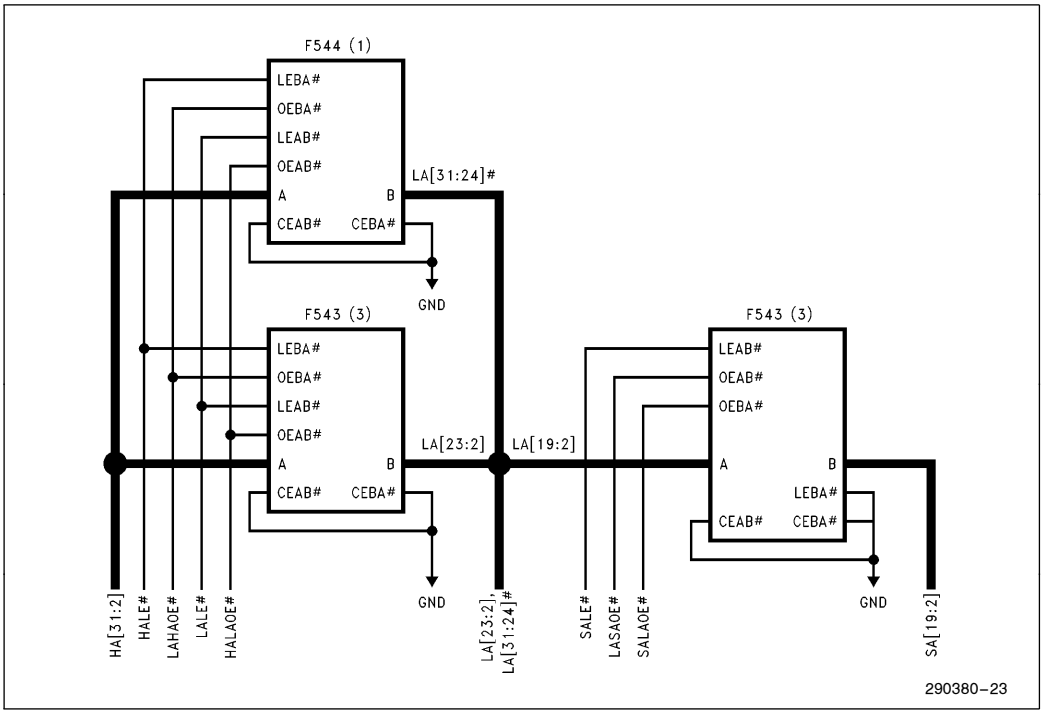


Figure 4-13. Discrete Representation of Address Buffer/Latch Logic

The following table summarizes the drive and latch functions of the address buffer/latch logic.

Table 4-12. Address Drive/Latch Functions

Signal	Cycle Type				
	HOST Master	EISA Master	ISA Master	DMA	REFRESH
HALAOE#	ACTIVE(1)	INACTIVE	INACTIVE	ACTIVE	ACTIVE
LASAOE#	ACTIVE	ACTIVE	INACTIVE	ACTIVE	ACTIVE
SALAOE#	INACTIVE	INACTIVE	ACTIVE	INACTIVE	INACTIVE
LAHAOE#	INACTIVE(2)	ACTIVE	ACTIVE	INACTIVE	INACTIVE
LALE#	LC	X	X	LO	LO
HALE#	LO	LO	LO	LO	LO
SALE#	LC	LC	LO	LC	LC

NOTES:
LC = Latch Closed: The latch is opened and then closed. On the rising edge of this signal, the address is latched.
LO = Latch Open: Latch is flow through for the entire cycle.
X = Don't care.
(1) When used in an 82350DT/enhanced system, this signal is inactive.
(2) When used in an 82350DT/enhanced system, this signal is active.

4.7 Byte Enable Translations (BE[3:0]#, HBE[3:0]#, SA0, SA1, and SBHE#)

The BE[3:0]#, HBE[3:0]#, SA0, SA1, and SBHE# are translated as shown in Table 4-13 and 4-14. Table 4-13 shows a translation from an ISA cycle to an EISA or host cycle. Table 4-14 shows a translation from a host or EISA cycle to an ISA cycle.

Table 4-13. Byte Enable Translations (ISA to EISA or HOST)

Input Signals			Output Signals
SBHE#	SA1	SA0	HBE[3:0]#/BE[3:0]#
0	0	0	1100
0	0	1	1101
0	1	0	0011
0	1	1	0111
1	0	0	1110
1	0	1	ILLEGAL
1	1	0	1011
1	1	1	ILLEGAL

Table 4-14. Byte Enable Translations (HOST or EISA or ISA)

Input Signals	Output Signals		
HBE[3:0]# or BE[3:0]#	SBHE#	SA1	SA0
1110	1	0	0
1101	0	0	1
1100	0	0	0
1011	1	1	0
1010	ILLEGAL		
1001	0	0	1
1000	0	0	0
0111	0	1	1
0110	ILLEGAL		
0101	ILLEGAL		
0100	ILLEGAL		
0011	0	1	0
0010	ILLEGAL		
0001	0	0	1
0000	0	0	0

4.8 HMI/O#, M-IO, HW/R#, and W-R Translations

The HMI/O#, M-IO, HW/R#, and W-R control signals are either inputs or outputs to the 82358DT, depending on the master in control of the bus and the system environment (i.e., 82350, 82350DT/buffered, or 82350DT/enhanced). These signals are translated and driven as shown in Table 4-15 through 4-19. Table 4-15 summarizes the 82358DT output buffer direction associated with these signals. Tables 4-16 through 4-19 breaks this down even further and shows which device or devices are responsible for driving each signal, and how the 82358DT translates them. Figures 4-14 through 4-16 show the system signal interconnects associated with each signal.

82350, 82350DT/Buffered Environment (AMODE = 0)(1)

Table 4-16 shows the relationship between HM/IO# and M-IO in both an 82350, and an 82350DT/buffered system environment.

Table 4-17 shows the relationship between HW/R# and W-R in both an 82350, and an 82350DT/buffered system environment.

Figure 4-14 shows how HM/IO#, M-IO, HW/R#, and W-R interconnect in an 82350 system.

Figure 4-15 shows how HM/IO#, M-IO, HW/R#, and W-R interconnect in an 82350DT/buffered system.

82358DT Output Buffer Direction Summary

Table 4-15. 82358DT Output Buffer Direction Summary

Signal	Bus Master	Signal Direction	
		AMODE = 0(1)	AMODE = 1(2)
HM/IO#	CPU	input	input
	DMA/Refresh	output	float
	EISA	float	float
	ISA	float	float
HW/R#	CPU	input	input
	DMA/Refresh	input	input
	EISA	output	float
	ISA	output	float
M-IO	CPU	input	input
	DMA/Refresh	input	output
	EISA	input	input
	ISA	output	output
W-R	CPU	output	float
	DMA/Refresh	output	float
	EISA	input	input
	ISA	output	output

NOTES:
1. AMODE = 0 = buffered configuration (82350 and 82350DT/buffered Systems)
2. AMODE = 1 = enhanced configuration (82350DT/enhanced Systems)

Table 4-16. HM/IO# and M-IO System Relationship

Signal	Bus Master	82358DT Signal Direction	Device Driving HM-IO#
HM/IO#	Host	Input	host master(2)
	DMA	Output	82358DT
	EISA	Float	EBB = M-IO(3)
	ISA	Float	EBB = M-IO(3)
Signal	**Bus Master**	**82358DT Signal Direction**	**Device Driving M-IO**
M-IO	Host	Input	EBB = HM/IO#(4)
	DMA	Input	EBB = HM/IO#(4)
	EISA	Input	EISA Master
	ISA	Output	82358DT = IORC# and IOWC#(5)

NOTES:
1. AMODE=0 = Buffer Mode (82350, and 82350DT/Buffered Systems)
2. In a 82350 system, the CPU drives HM/IO#. In an 82350DT system, the 82359 DRAM controller drives HM/IO#
3. M-IO is propagated through the EBB and driven as HM/IO#. For ISA master cycles, the 82358DT translates IORC# and IOWC#, and outputs them as M-IO.
4. HM/IO# is propagated through the EBB and driven as M/IO
5. The 82358DT translates IORC# and IOWC#, and outputs them as M-IO

Table 4-17. HW/R# and W-R System Relationship

Signal	Bus Master	82358DT Signal Direction	Device Driving HW/R#
HW/R#	Host	Input	Host Master
	DMA	Input	82357 (ISP)
	EISA	Output	82358DT = W-R(2)
	ISA	Output	82358DT = ISARWCMD(3)
Signal	**Bus Master**	**82358DT Signal Direction**	**Device Driving W-R**
W-R	Host	Output	82358DT = HW/R#(4)
	DMA	Output	82358DT = HW/R#(4)
	EISA	Input	EISA Master
	ISA	Output	82358DT = ISA RW CMD(5)

NOTES:
1. AMODE=0 = 82350, and 82350DT/buffered Systems
2. W-R is propagated through the 82358DT and driven as HW/R#
3. The ISA read and write command signals (MRDC#, MWTC#, IORC#, IOWC#) are translated by the 82358DT and driven as HW/R#
4. HW/R# is propagated through the 82358DT and driven as W-R
5. The ISA read and write command signals (MRDC#, MWTC#, IORC#, IOWC#) are translated by the 82358DT and driven as W-R

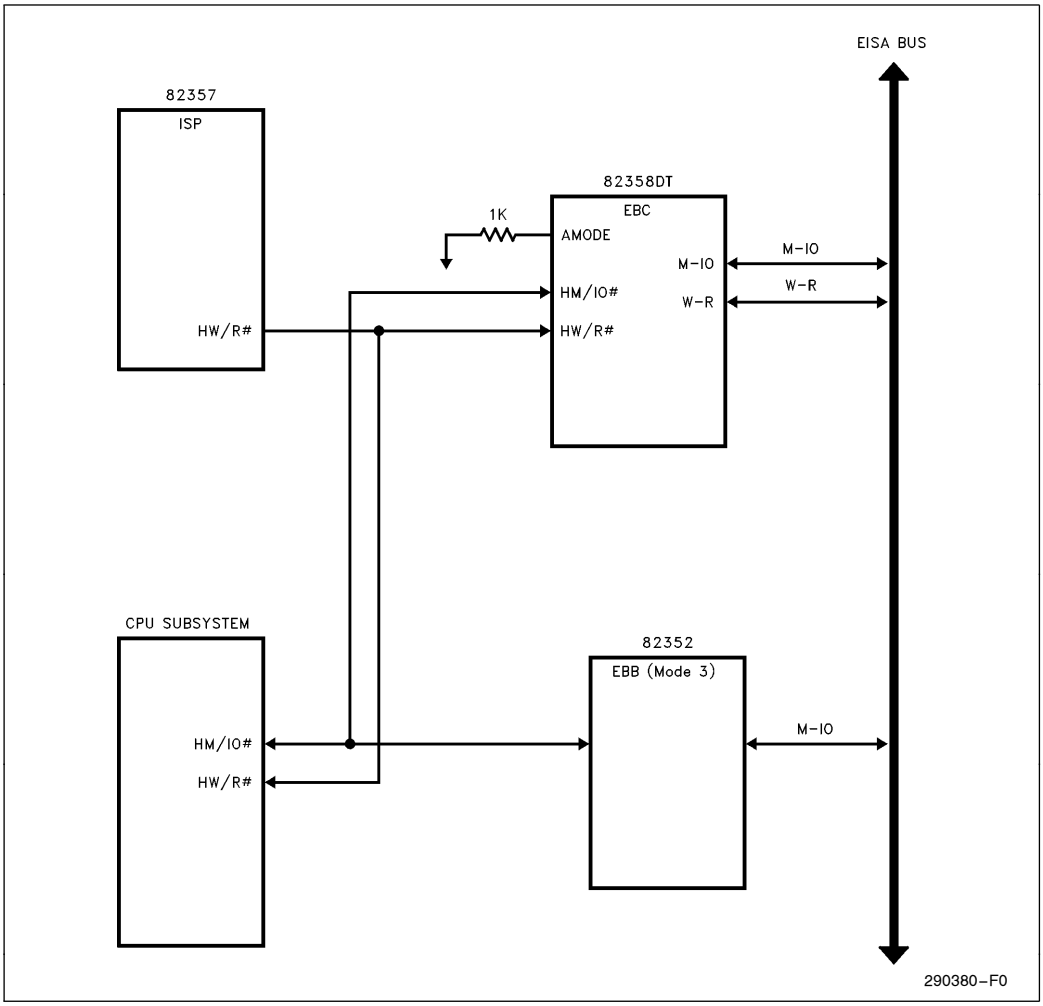


Figure 4-14. HM/IO#, M-IO, HW/R#, and W-R System Interconnects (82350 Configuration)

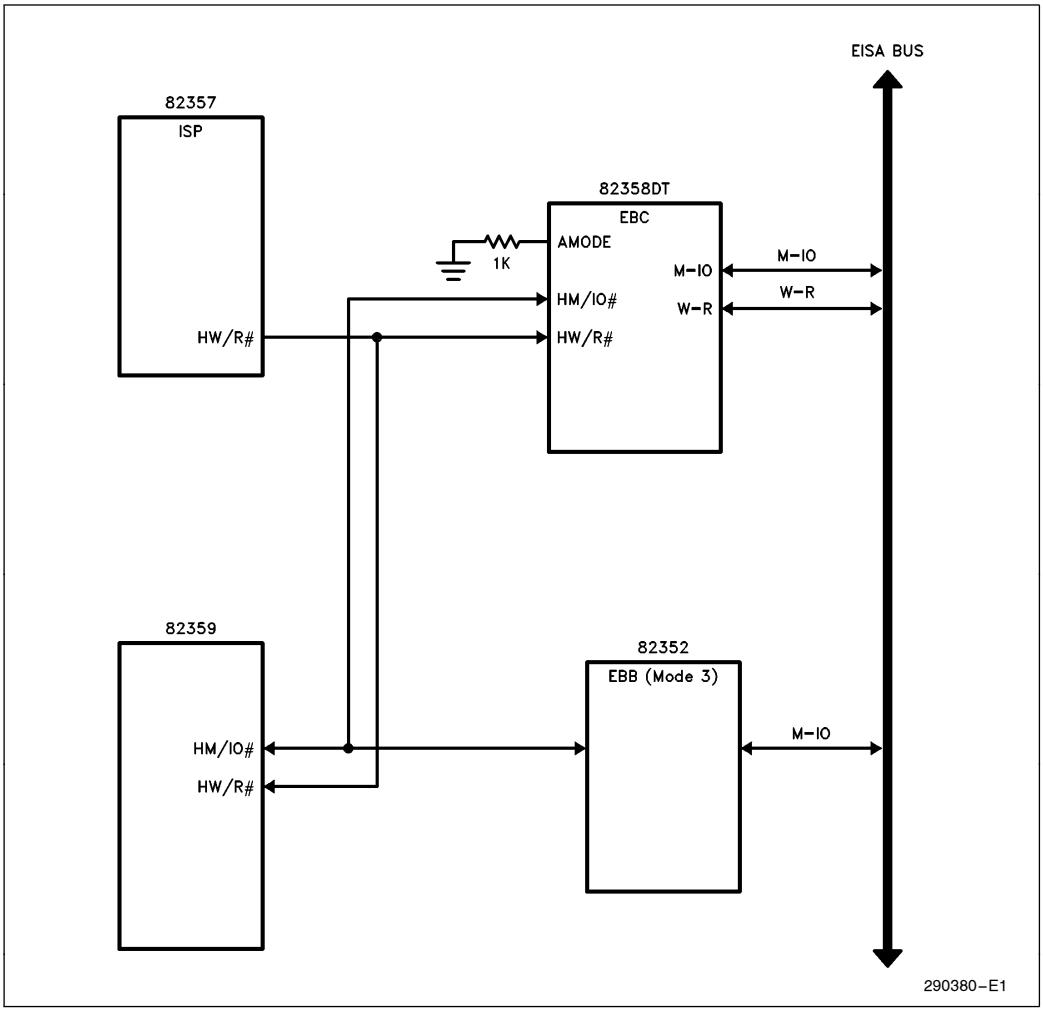


Figure 4-15. HM/IO#, M-IO, HW/R#, and W-R System Interconnects (82350DT/buffered Configuration)

82350DT/Enhanced HM/IO# and M-IO Translation (AMODE = 1)(1)

Table 4-18 shows the relationship between HM/IO# and M-IO in an 82350DT/enhanced system environment.

Table 4-19 shows the relationship between HW/R# and W-R in an 82350DT/enhanced system environment.

Figure 4-16 shows how HM/IO#, M-IO, HW/R#, and W-R interconnect in an 82350DT/enhanced system.

Table 4-18. 82358DT HM/IO# and M-IO System Relationship

Signal	Bus Master	82358DT Signal Direction	Device Driving HM-IO#
HM/IO#	Host	Input	82359
	DMA	Float	(2)
	EISA	Float	(3)
	ISA	Float	(4)
Signal	**Bus Master**	**82358DT Signal Direction**	**Device Driving M-IO**
M-IO	Host	Input	82359
	DMA	Output	82358DT
	EISA	Input	EISA Master
	ISA	Output	82358DT(5)

NOTES:
1. AMODE = 1 = 82350DT/enhanced Systems
2. The 82358DT drives M-IO high during DMA cycles. M-IO is tied directly to the 82359's SM/IO# input.
3. The current EISA Master drives M-IO during EISA master cycles. M-IO is tied directly to the 82359's SM/IO# input.
4. The current ISA Master's IORC# and IOWC# control signals are translated by the 82358DT and output as M-IO. M-IO is tied directly to the 82359's SM/IO# input.
5. The ISA master memory and I/O control signals (IORC# and IOWR#) are translated by the 82358DT and output as M-IO.

Table 4-19. HW/R# and W-R System Relationship

Signal	Bus Master	82358DT Signal Direction	Device Driving HW/R#
HW/R#	Host	Input	82359
	DMA	Input	82357 (ISP)(6)
	EISA	Float	EISA Master, EBB = W-R(2)
	ISA	Float	82358DT, EBB = W-R(3)
Signal	**Bus Master**	**82358DT Signal Direction**	**Device Driving W-R**
W-R	Host	Float	82359
	DMA	Float	EBB = HW/R#(4)
	EISA	Input	EISA Master
	ISA	Output	82358DT(5)

NOTES:
1. AMODE = 1 = 82350DT/Enhanced Systems
2. W-R is propagated through the EBB and driven as HW/R# for ISP accesses. W-R is tied directly to the 82359's SW/R# input and used during host accesses.
3. The ISA read and write command signals (MRDC#, MWTC#, IORC#, IOWC#) are translated by the 82358DT and driven directly to the 82359's SW/R# and EBB inputs as W-R. W-R is propagated through the EBB as HW/R# for ISP accesses.
4. HW/R# is propagated through the EBB and driven as W-R.
5. The ISA read and write command signals (MRDC#, MWTC#, IORC#, IOWC#) are translated by the 82358DT and driven as W-R.
6. HW/R is driven by the ISP, propagated through the 82358DT and driven as W-R. W-R is tied directly to the 82359's SW/R# input and used during host accesses.

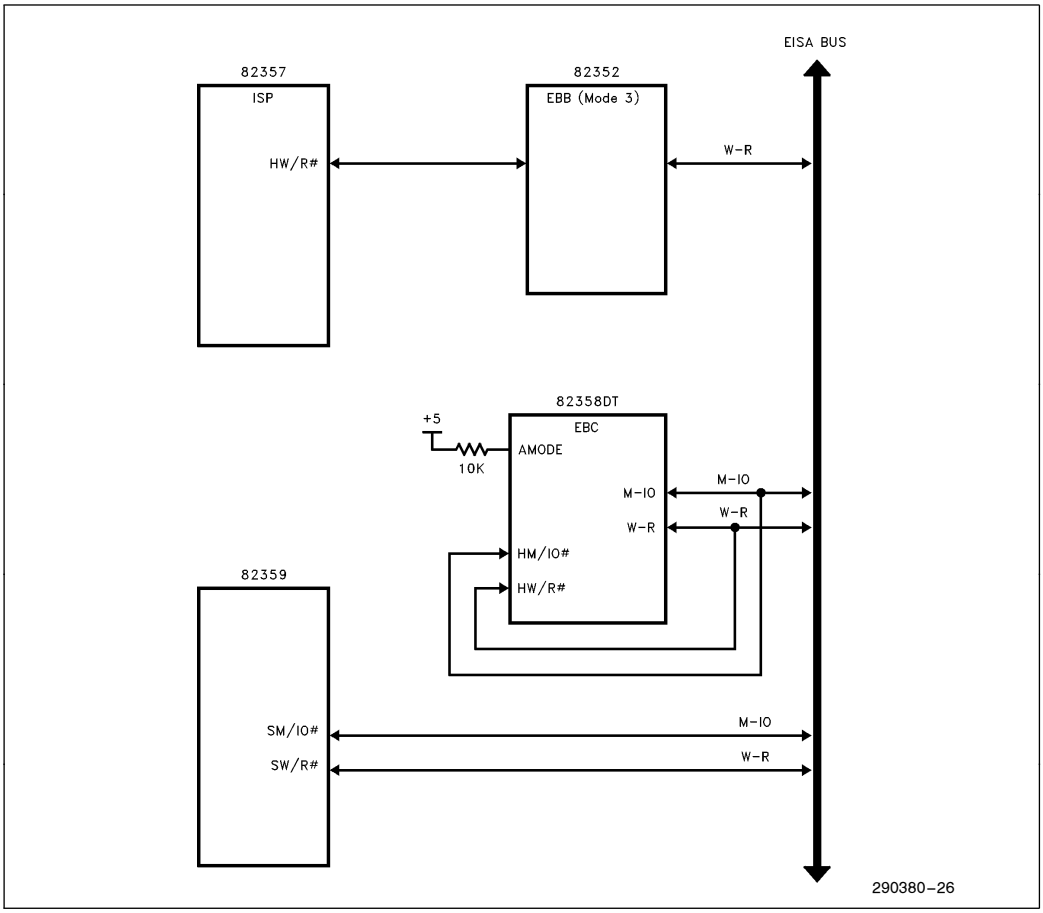


Figure 4-16. HM/IO# and M-IO Interconnects (82350DT/Enhanced Configuration)

4.9 BCLK Stretching

The high or low time of BCLK is stretched as indicated by the following three events:

1) End of cycle during CMD# on the EISA bus when HSTRETCH# is sampled active (refer to Figure 4-17). This results in extending the cycle by holding BCLK and CMD# low until HSTRETCH# has been sampled inactive. After being sampled active, HSTRETCH is sampled on every other HCLKCPU rising edge for 386 systems (CLK1 intervals) and every HCLKCPU rising edge for i486 systems, until it is sampled inactive. HSTRETCH# should not be driven active until CMD# is driven active, and should not remain active for more than 400ns. To prevent HSTRETCH# from being driven active while CMD# is inactive, gate HSTRETCH# with CMD# active. HSTRETCH# can be used to extend a cycle during EISA master and DMA/refresh cycles to host slaves only. It is not recommended to stretch BCLK during ISA master cycles (including ISA master initiated refresh), as ISA masters can be asynchronous to BCLK.
2) When a Host bus master is accessing an EISA or ISA slave, the rising edge of BCLK is synchronized to the falling edge of CMD# (refer to Figures 4-18, 4-20, and 4-21).
3) When an ISA master is accessing an EISA or HOST slave (EISA translation performed), the rising edge of BCLK is synchronized to the falling edge of CMD# (refer to Figures 4-19 through 4-21).

NOTE:
As a result of stretching BCLK under conditions two and three above, BCLK may not have a falling edge during the duration of START#. Events that are synchronized to BCLK edges should be done without regard to frequency or duty cycle.

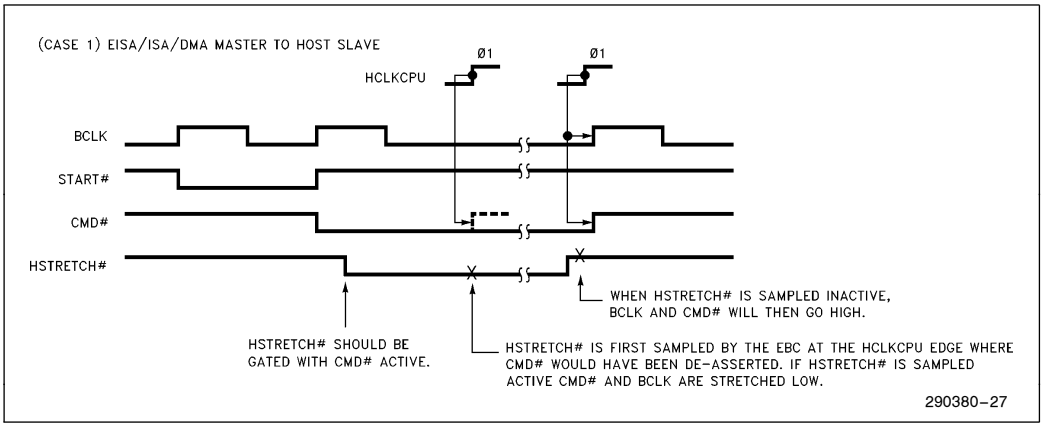


Figure 4-17. BCLK Stretching Caused by HSTRETCH#

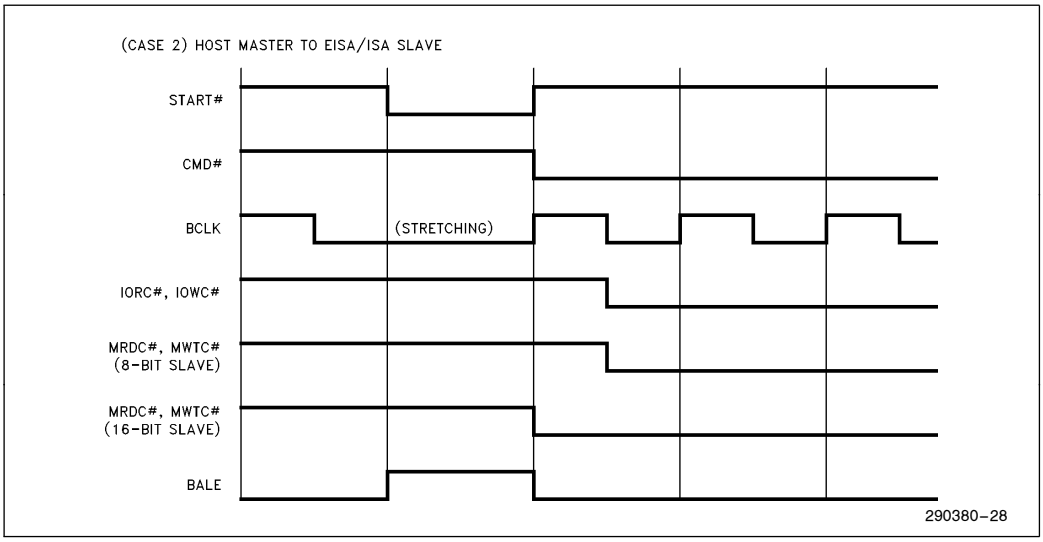


Figure 4-18. BCLK Stretching During Host Master to EISA/ISA Slave Cycles

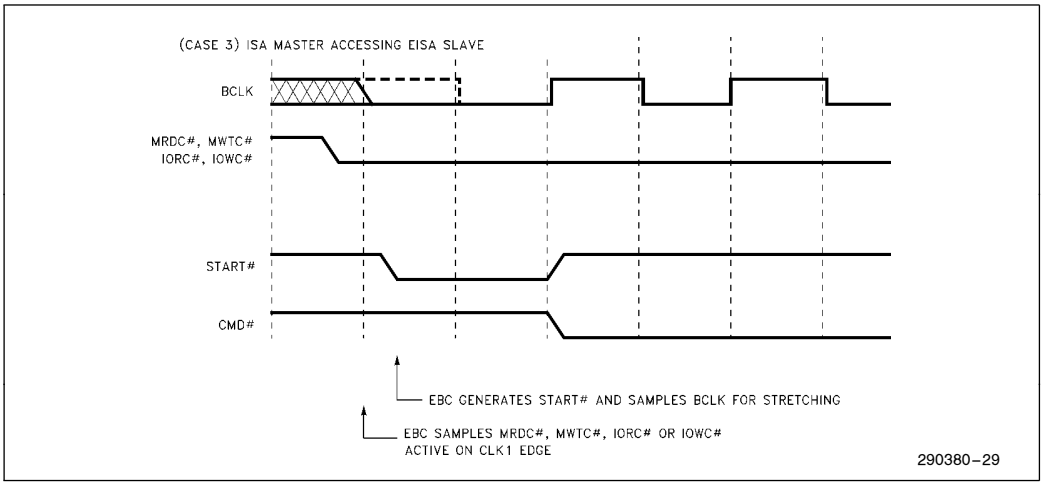
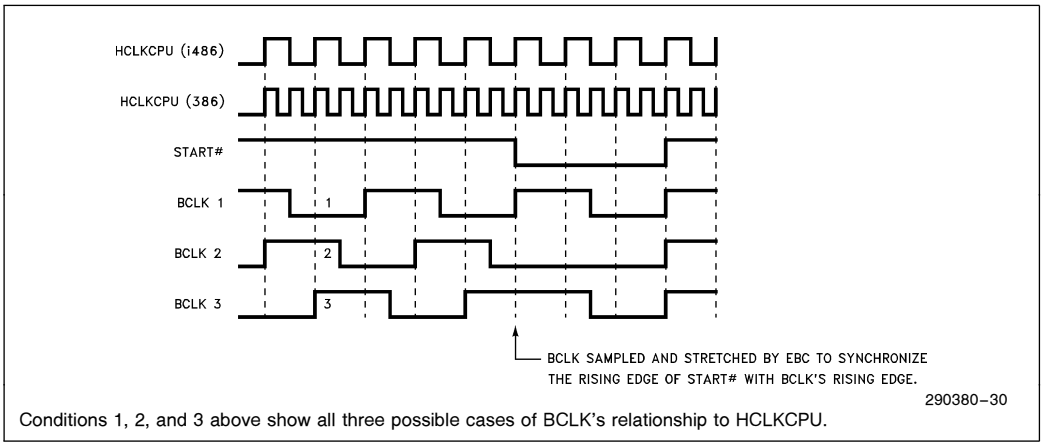


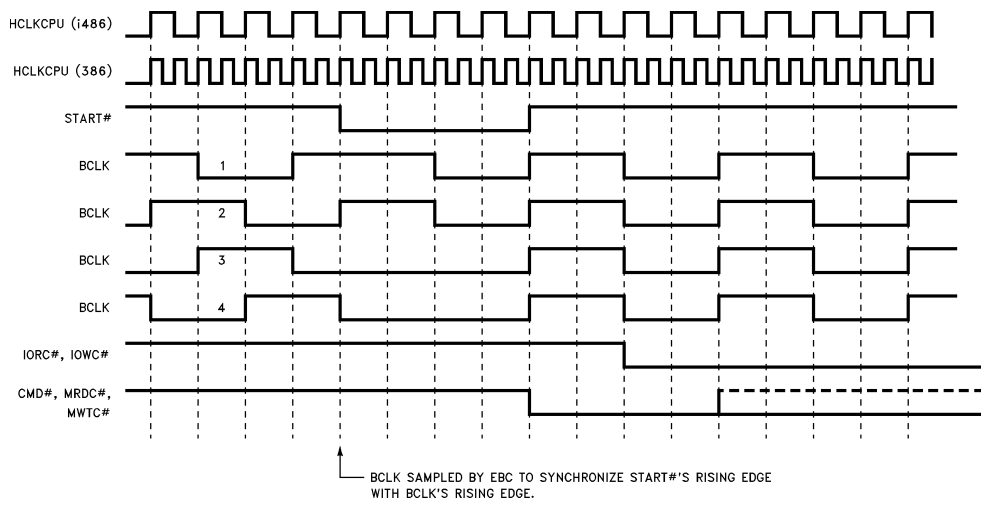
Figure 4-19. BCLK Stretching During ISA Master to EISA or HOST Slave Cycles

Figures 4-20 and 4-21 illustrate the relationship of HCLKCPU and START# to BCLK as related to conditions two and three above.



Conditions 1, 2, and 3 above show all three possible cases of BCLK's relationship to HCLKCPU.

Figure 4-20. BCLK Stretching 25 MHz 386 & i486 CPUs



Conditions 1, 2, 3, and 4 show all four possible cases of BCLK's relationship to HCLKCPU.

Figure 4-21. BCLK Stretching 33 MHz 386 & i486 CPUs

4.10 I/O Recovery Support

The 82358DT automatically forces a minimum of one BCLK delay between back to back 8-bit and 16-bit ISA I/O cycles originating on the host bus. The delay is measured from the trailing edge of I/O command (IORC# or IOWC#) to the leading edge of the next START#.

If a delay of greater than one BCLK is desired, LIOWAIT can be asserted to provide a maximum delay of 11 BCLKs for 8-bit I/O devices or three BCLKs for 16-bit I/O devices. Delays in between the minimum and maximum delay are controlled by the deassertion of LIOWAIT#.

LIOWAIT# is sampled on the rising edge of the I/O command strobe (IORC# or IOWC#). If LIOWAIT# is sampled active, the START# signal of the next cycle is delayed until LIOWAIT# is sampled inactive.

No delay is inserted for back to back I/O ''sub-cycles'' generated as a result of byte assembly or disassembly.

Figure 4-22 shows the general function of LIOWAIT#, standard one BCLK delay, and maximum delay for a 16-bit ISA slave. Figure 4-23 shows the maximum BCLK delay for an 8-bit ISA slave.

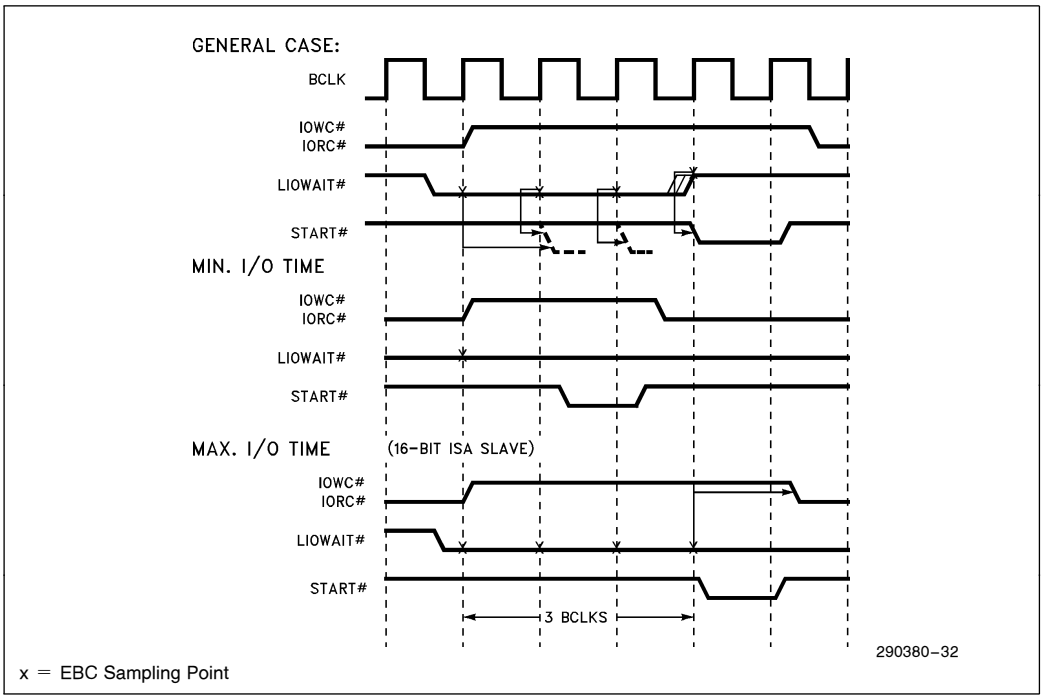


Figure 4-22. Maximum BCLK Delay for a 16-Bit ISA Slave

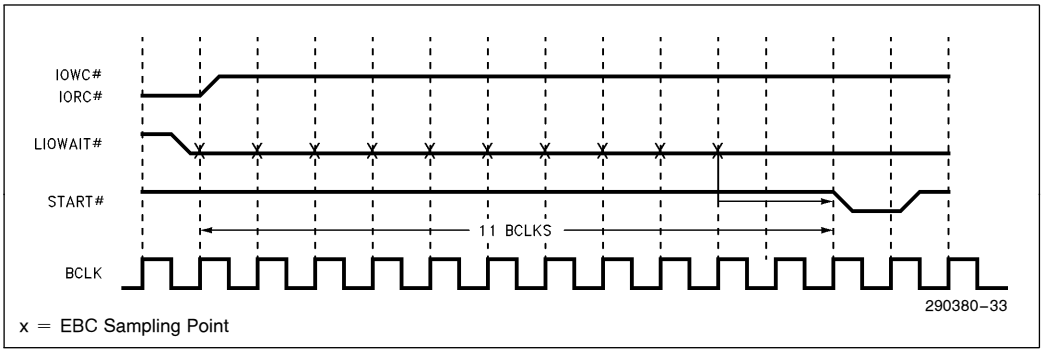


Figure 4-23. Maximum BCLK Delay for an 8-Bit ISA Slave

4.11 Snoop Support

The 82358DT provides two signals (HSSTRB# and QHSSTRB#) for the purpose of bus snooping. HSSTRB# is used in 82350(386/82385) systems and QHSSTRB# is used in 82350(i486) and 82350(386/82395) systems. In 82350DT systems, bus snooping is provided by the 82359 DRAM controller. Both HSSTRB# and QHSSTRB# are defined as ''No Connect'' pins when used in an 82350DT system.

These signals indicate to a system cache controller that a bus master is writing to system memory. They are used by the cache controller to maintain data coherency between system memory and cache memory.

Figures 4-24 through 4-26 show the snoop strobe timing for HOST, EISA, and DMA master cycles. During DMA and EISA master non-burst cycles, HSSTRB# and QHSSTRB# are generated for one CLK1 duration after START# is driven inactive. For additional basic function timing information, refer to section 5.0.

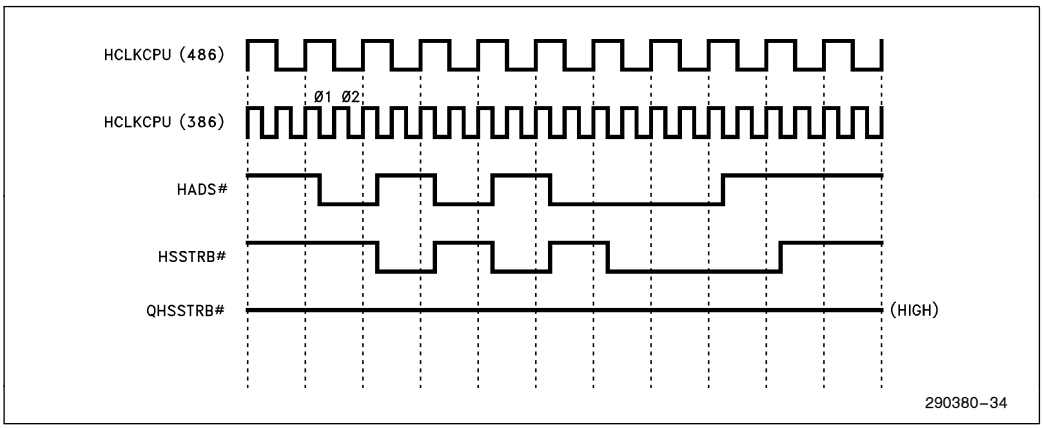


Figure 4-24. Host Master to Host Memory Timing

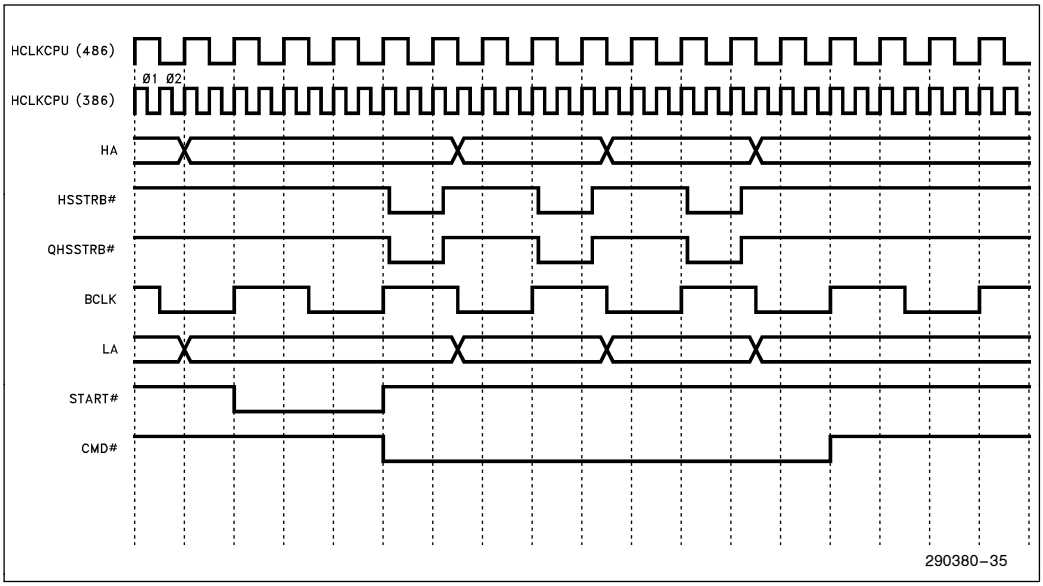


Figure 4-25. EISA Master Burst or DMA Burst Timing to Host Memory (25 MHz)

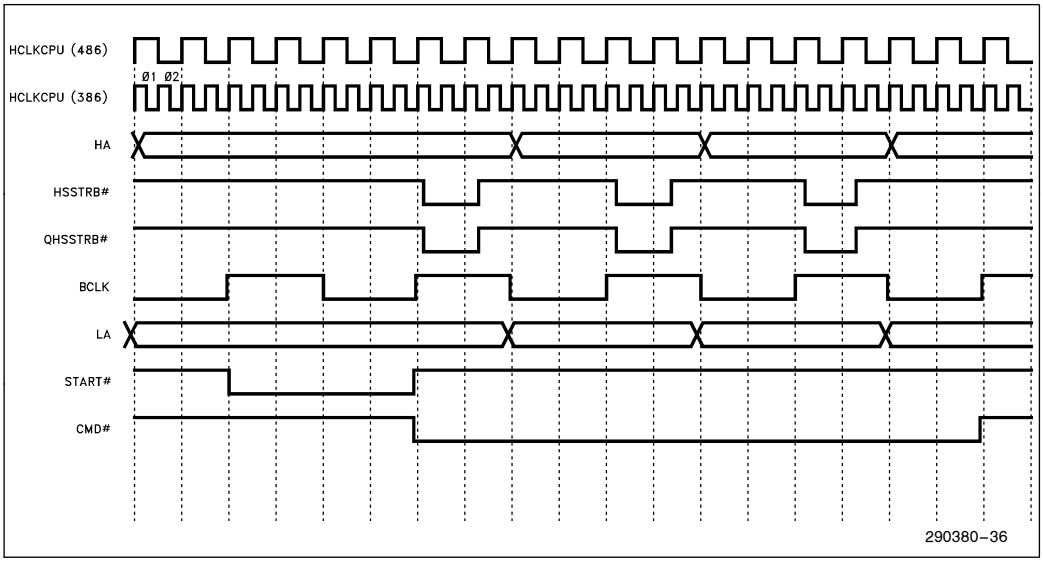


Figure 4-26. EISA Master Burst or DMA Burst Timing to Host Memory (33 MHz)

4.12 Address Pipelining Support

Address pipelining is supported in 82350/386 systems only. In 82350/i486 and 82350DT system environments, address pipelining is not used. Address pipelining allows the next address and cycle definition signals to be placed on the bus prior to the completion of the current cycle. Pipelined address timing reduces wait state requirements and allows the EISA or ISA cycle to run as back-to-back cycles on the EISA/ISA bus.

A Host Next Address (HNA#) output is provided to indicate to the Host bus CPU that a new address (A2–A31 and HBE[3:0]#), and cycle definition (HW/R#, HD/C#, and HM/IO#) can be placed on the bus. Specifically, HNA# is pulsed active for one CLK1 period, indicating that the address has been latched and can be changed.

Figure 4-27 shows a functional timing illustration of HNA#. Refer to the host basic function timings, section 5.2, for additional timing information.

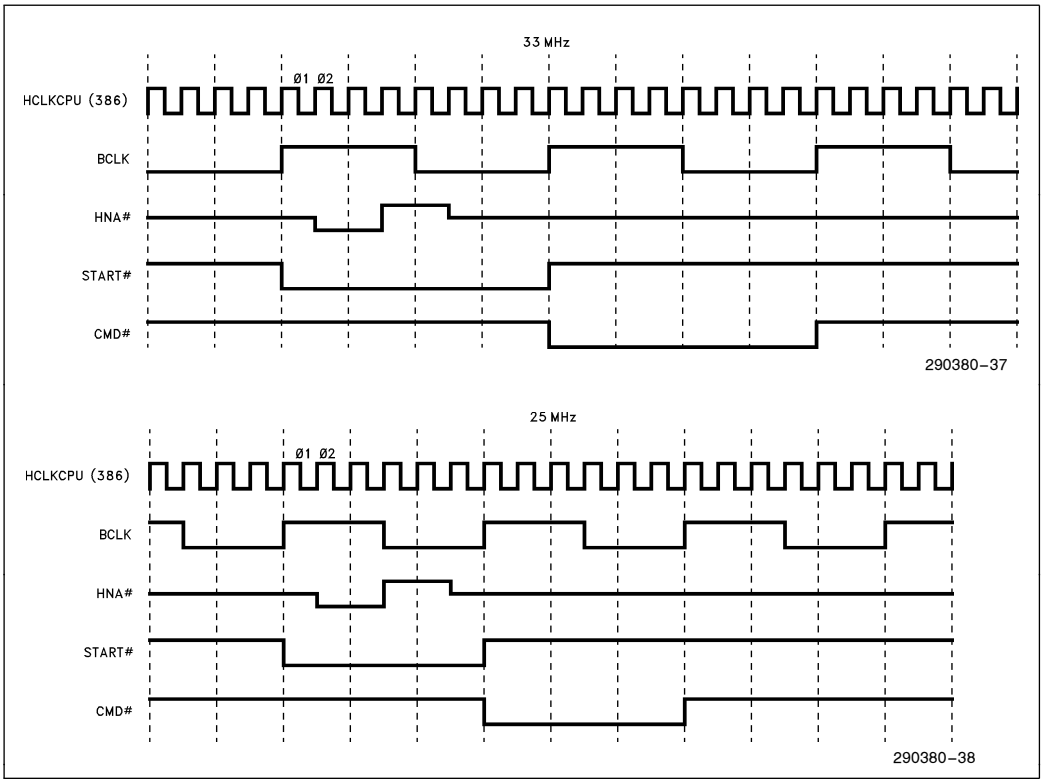


Figure 4-27. HNA# Timing

4.13 Locked Cycle Support

The 82358DT provides lock cycle support by propagating the CPU or host master HLOCK# signal to the EISA bus as LOCK#. Locked cycles are run to guarantee exclusive host master to EISA/ISA memory accesses during the time LOCK# is active.

If HLOCK# is sampled active on the rising edge of HCLKCPU at the end of START#, LOCK will be driven active. LOCK# will remain active until HLOCK# is sampled inactive on the rising edge of HCLKCPU, where START# is asserted, during an unlocked pipelined cycle that was preceded by a locked posted write cycle (refer to Figure 4-31), or on the rising edge of HCLKCPU (at BLCK rising) that HLOCK#, START#, and CMD# are sampled inactive for subsequent unlocked pipelined and idle cycles (refer to Figures 4-30 and 4-32). LOCK# will remain active as long as HLOCK# is active.

NOTE:
Extra lock cycles will be generated under the following conditions: Condition 1 applies to any 82350 or 82358DT based system. Condition 2 applies to 82350/386 (with or without cache) based systems only.

(1) During transfers where a posted write cycle directly precedes a locked cycle, the posted write cycle will also be locked. In this case, HLOCK# is driven active prior to or during the START# signal corresponding to the posted write cycle. As mentioned above, LOCK# is asserted if HLOCK# is sampled active at the rising edge of HCLKCPU at the end of START# (refer to Figure 4-28).

(2) If the cycle following a locked cycle is pipelined, the pipelined cycle will also be locked. The 82358DT runs host pipelined cycles as back-to-back cycles on the EISA bus (i.e., there is no idle time between the last CMD# and the next START#).

During the pipelined cycle, the falling edge of HLOCK# does not occur until after the falling edge of START# (refer to Figure 4-29). To negate LOCK#, HLOCK# must be negated before START# is driven low.

4.14 Halt, Flush, Write Back, Shutdown Cycle Support

The 82358DT terminates halt, flush, and write back cycles by generating either HERDYO# and HRDYO#, or ARDY, depending on the system environment (82350 or 82350DT). These cycles are decoded as shown in Table 4-20. Figures 5-70 and 5-71 show a halt/flush/write back cycle sequence.

Table 4-20. Halt, Flush, Write Back Cycle Decode

CPU	HM/IO#	HD/C#	HW/R#	HBEO#
80386	1	0	1	1
80486	0	0	1	1

NOTE:
Flush and Write Back cycles apply to 80486 systems only.

The 82358DT supports shutdown cycles by generating either HERDYO#, HRDYO#, RSTCPU, and RST385 or ARDY, RSTCPU, and RST385, depending on the system environment (82350 or 82350DT). A shutdown cycle is decoded as shown in Table 4-21. Figures 5-70 and 5-71 show a shutdown cycle sequence.

Table 4-21. Shutdown Cycle Decode

CPU	HM/IO#	HD/C#	HW/R#	HBEO#
80386	1	0	1	0
80486	0	0	1	0

NOTE:
EISA and ISA cycles are not generated during halt, flush, write back, and shutdown cycles.

4.15 Slot Support

The slot support provided by the 82358DT includes the generation of a latch enable signal (AENLE#) used to control the latching of the slot specific AENx (x = slot number) signals during transfers. The AENx signals are used by slave devices to determine if they can respond to addresses and I/O commands on the bus. These signals are generated by external logic and are latched on the rising edge of AENLE# and remain latched until AENLE# is driven active. Figure 4-33 shows the generation of AENLE# by master type.

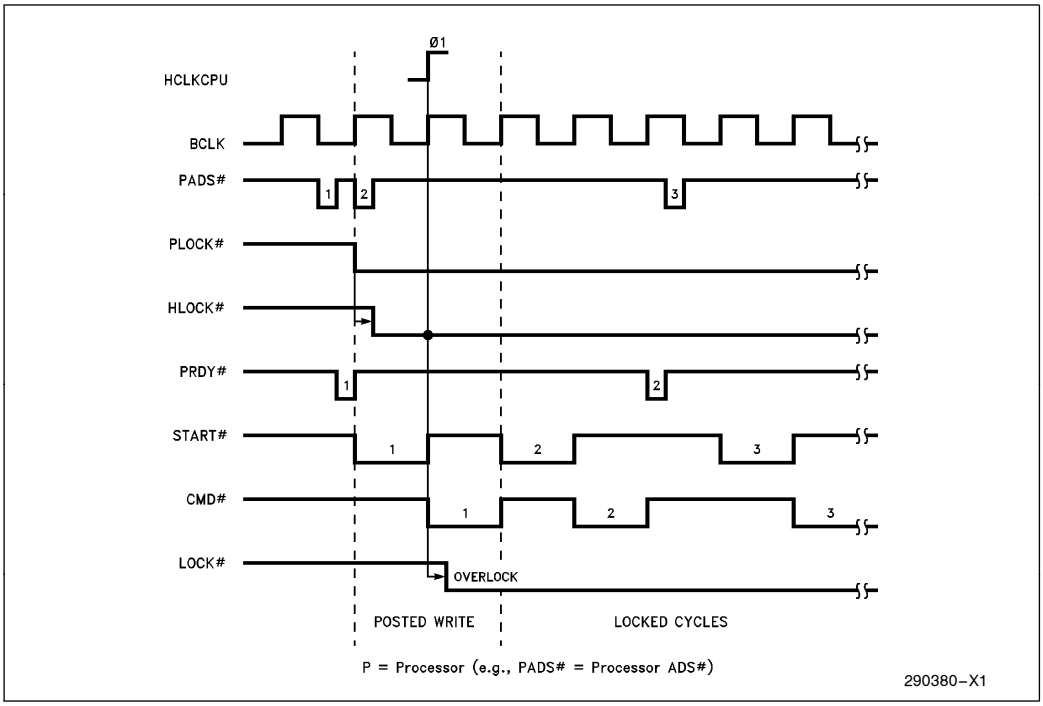


Figure 4-28. Overlock Case 1 (82350 System used as Example)

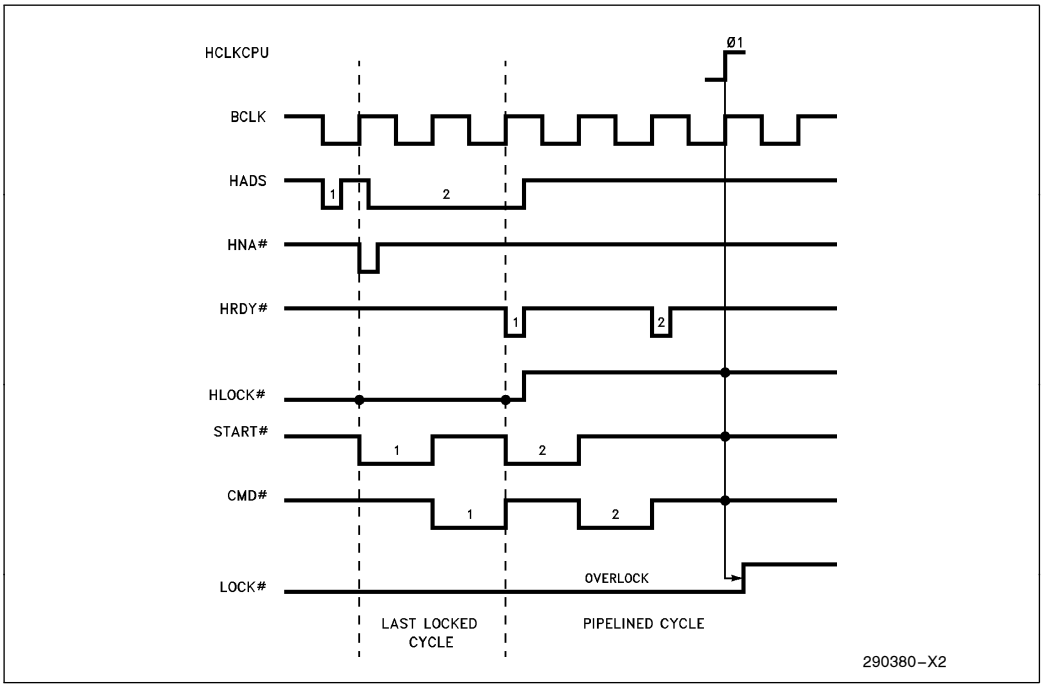


Figure 4-29. Overlock Case 2 (82350/386 System)

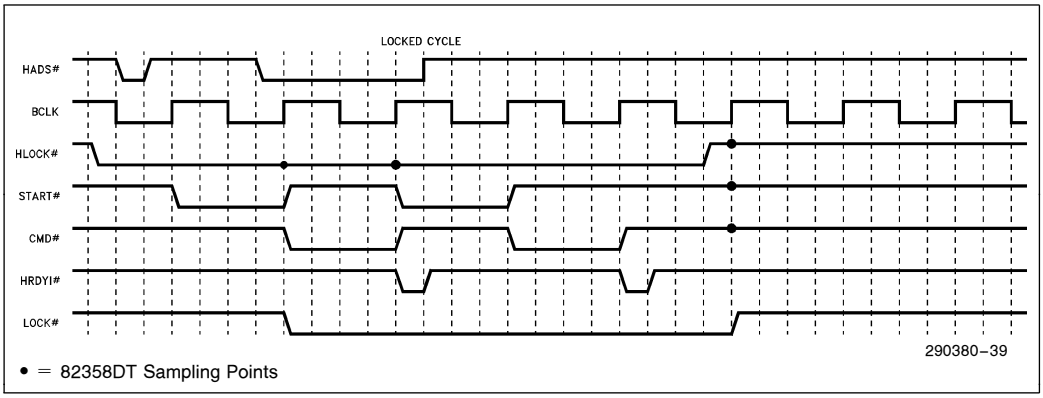
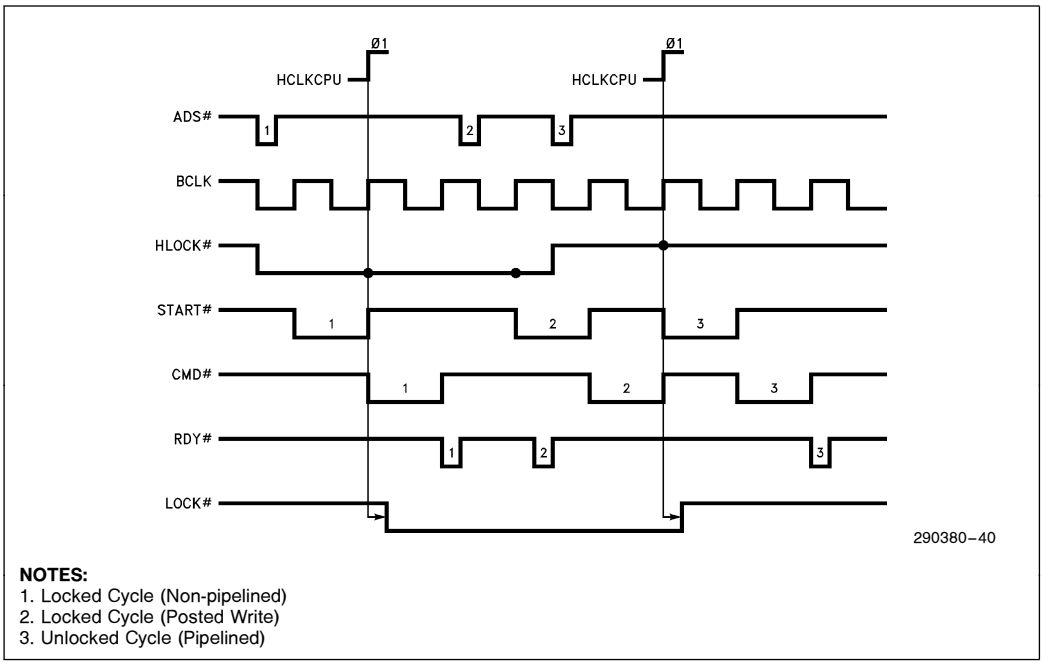


Figure 4-30. Host Master Lock Cycle to EISA Slave (82350/386 Pipelined)



NOTES:
1. Locked Cycle (Non-pipelined)
2. Locked Cycle (Posted Write)
3. Unlocked Cycle (Pipelined)

Figure 4-31. Host Master Lock Cycle to EISA Slave

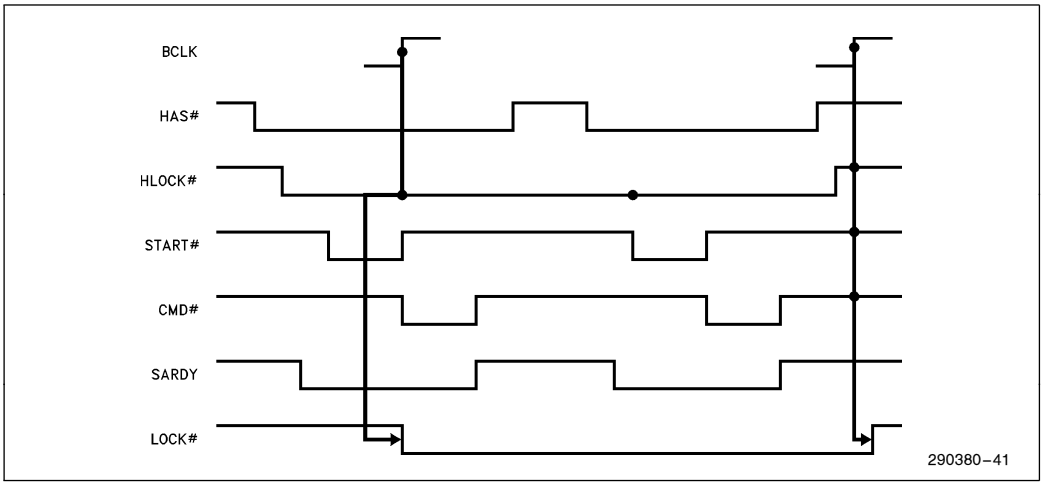


Figure 4-32. Host Master Lock Cycle to EISA Slave (82350DT/386 or i486)

For ISA slave assembly, disassembly, or i486™ burst cycles, AENLE# will remain inactive for all subsequent cycles within the assembly/disassembly or i486 burst process.

AENLE# is driven active (low) from the rising edge of HHLDA and remains low as long as HHLDA is active (high). When transitioning from an EISA master, ISA master, or DMA cycle to a CPU cycle, AENLE# remains low until the falling edge of BCLK during the START# that is caused by the CPU cycle.

4.16 Clock Generation

The 82358DT generates BCLK, CLKKB, and the 82358DT internal CLK1 (EBC__CLK1) from HCLKCPU input. EBC__CLK1's relationship to HCLKCPU in an 80386 system and i486 system is shown in Figure 4-34.

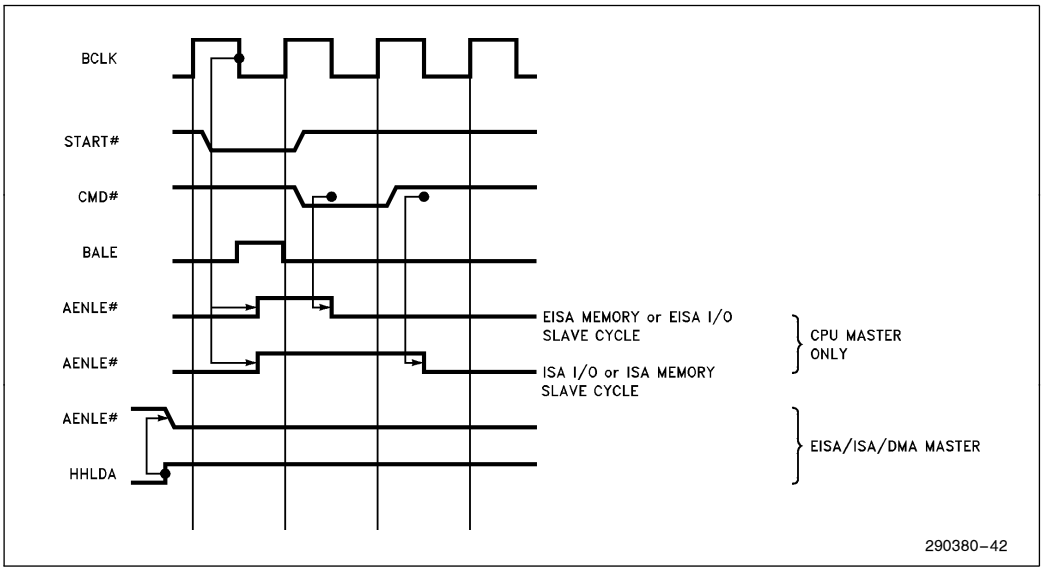


Figure 4-33. AENLE# Timing Diagram

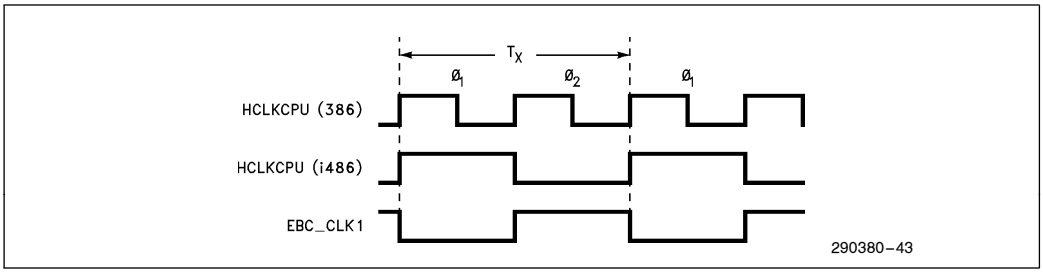


Figure 4-34. EBC__CLK1 and HCLKCPU Relationship

4.17 Bus Cycle Definition (HD/C#, HMI/O#, and HW/R)

The EBC decodes HMI/O#, HD/C#, HW/R#, and HBE0# as shown in Table 4-22 to determine the type of bus cycle being performed.

Table 4-22. Cycle Definition (HD/C#)

HM/IO#	HD/C#	HW/R#	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Halt/Shutdown(1,2)
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Code Read
1	0	1	Reserved(1,2)
1	1	0	Memory Read
1	1	1	Memory Write

NOTES:
1. In an 80386 system environment, the Halt/Shutdown cycle bus definition is (101), and bus definition (001) is reserved. In an 80486 system environment, Halt and Shutdown are defined as shown in the above table.
2. The 82358DT samples HBE0# at the start of a halt/shutdown cycle to determine if the cycle is a halt or shutdown cycle.

Halt	Shutdown
HBE0# = 1	HBE0# = 0

5.0 CYCLE TYPES (BASIC FUNCTION WAVEFORMS)

The following section provides the basic function timings associated with the 82358DT. The timing waveforms are broken down into six different categories: (category 1) 82350 host cycles, (category 2) 82350DT host cycles, (category 3) EISA master cycles, (category 4) ISA master cycles, (category 5) DMA cycles, and (category 6) miscellaneous or special cycles.

5.1 Guide Lines When Reading the Basic Function Waveforms

When reading the basic function timing waveforms, use the following as a guide line:

(1) The basic function timing waveforms, Figures 5-1 through 5-55 and 5-70 through 5-75, are test simulations. These simulations do not include any valid delays, float delays, or propagation delays normally associated with the 82358DT's outputs (i.e., the transition of an output will occur concurrently with the specific edge of the clock or signal from which this output is caused).

The inputs to the 82358DT are generated to guarantee set-up and hold times. In some cases the input signal may be active or valid throughout the entire diagram (e.g., MASTER16# during ISA master cycles). And in some cases, the input may just surround the specific clock edge from which the input is sampled (e.g., HADS# surrounds the falling edge of EBC__CLK1 during 82350 host master cycles).

(2) The CLK1 signal represented in all six categories of the timings is the internal CLK1 of the 82358DT (EBC__CLK1). The relationship of EBC__CLK1 to HCLKCPU (386 and i486) is shown in Figure 4-34.

(3) Some of the signals have been bused or combined together. There are three different methods for busing (type "a", type "b", and type "c").

Type "a" signal name[value:value]–When reading a type"a" bused signal, the following example can be used: BE[3:0]# is a bused version of BE3#, BE2#, BE1#, and BE0#. In a timing, a value of 0001 associated with BE[3:0]# is read from left to right starting with BE3# (i.e., BE3# = 0, BE2# = 0, BE1# = 0, and BE0# = 1).

Type "b" signal name, signal name–When reading a type "b" bused signal, the following example can be used: WR,MIO is a bused version of the EISA signals W-R and M-IO. In a timing, a value of 01 associated with WR,MIO is read from left to right starting with W-R (i.e., W-R = 0 and M-IO = 1).

Type "c" signal name[signal identifier:signal identifier]–When reading a type "c" bused signal, the following example can be used: HLOC[M:IO] is a bused version of HLOCMEM# and HLOCIO#. In a timing, a value of 01 associated with HLOC[M:IO] is read from left to right starting with HLOCMEM# (i.e. HLOCMEM# = 0 and HLOCIO# = 1).

(4) AMODE = 0 for all of the basic function waveforms.

5.2 82350 Host Master Cycles

If the Host, EISA, and ISA buses are not currently owned by a bus master, the host CPU has default access (i.e. access is automatic and it is not necessary to gain access through the system arbiter [ISP]). However, if the bus is currently owned by a master, the host CPU must gain access to the EISA/ISA bus through the ISP. This is done via the ISP's CPUMISS# line.

[1]The beginning of an 82350 host cycle starts when the 386 or i486 drives HADS# active, indicating that the address, HBE[3:0]#, HM/IO#, HW/R#, and HD/C# are valid on the host bus. The 82358DT then samples HLOCMEM# and HLOCIO# to determine if the host cycle needs to be forwarded to the EISA/ISA bus.

[2]If the host master cycle is a memory cycle and HLOCMEM# is sampled inactive, or the host master cycle is an I/O cycle and HLOCIO# is sampled inactive, the 82358DT will generate the EISA/ISA command signals and Host Next Address (HNA#). HNA# is driven active for one EBC__CLK1 period to support 386 pipelining (refer to section 4.12). At the end of the cycle on the EISA/ISA bus, the 82358DT will drive HERDYO# active, followed an EBC__CLK1 later, by HRDYO#, indicating to the host CPU that the transfer is complete. The 82358DT provides all the data swap control if data size translation is necessary. The 82358DT determines if data size translation is necessary by sampling the slave and master decode signals at the start of the transfer (refer to section 4.3).

Any host cycle to the EISA/ISA bus can be extended by driving either EXRDY (EISA slave) or CHRDY (ISA slave) low. The number of wait states added depends on how long EXRDY or CHRDY are held low (refer to Table 4-6).

If a posted memory write cycle is indicated (PWEN# active), the 82358DT will terminate the cycle on the host bus by driving HERDYO# active after the host data has been latched on the rising edge of HDSDLE1#. The 82358DT will then complete the cycle on the EISA/ISA bus. For additional information, refer to section 4.1.3.

NOTES:

(1) The 82358DT controls the propagation of the HA[31:2] address through the address buffers onto the LA[31:2] and SA[19:2] buses. The 82358DT also translates the HBE[3:0]# lines to SA0, SA1, SBHE#, and BE[3:0]#, and HW/R# to W-R. MI/O is propagated to the EISA bus along with the address lines.

(2) If the cycle is directed to an EISA slave, only the EISA command signals will be generated (START# and CMD#). If the cycle is directed to an ISA slave, both the EISA command signals and the ISA command signals (IORC#, IOWC#, MRDC#, and MWTC#, depending on the slave type, will be generated. Please refer to Table 4-9.

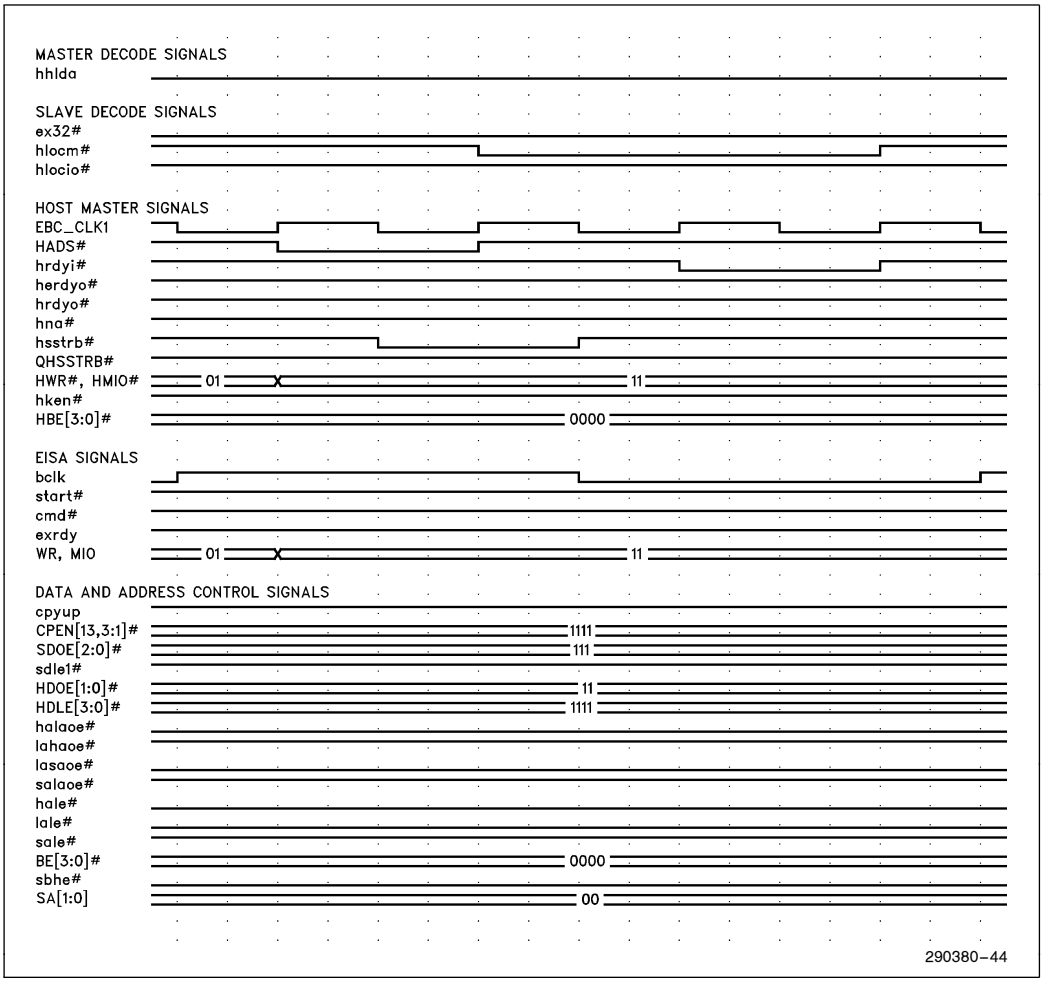


Figure 5-1. Host Master to Host Memory Slave Standard Write Cycle-Four Byte Transfer

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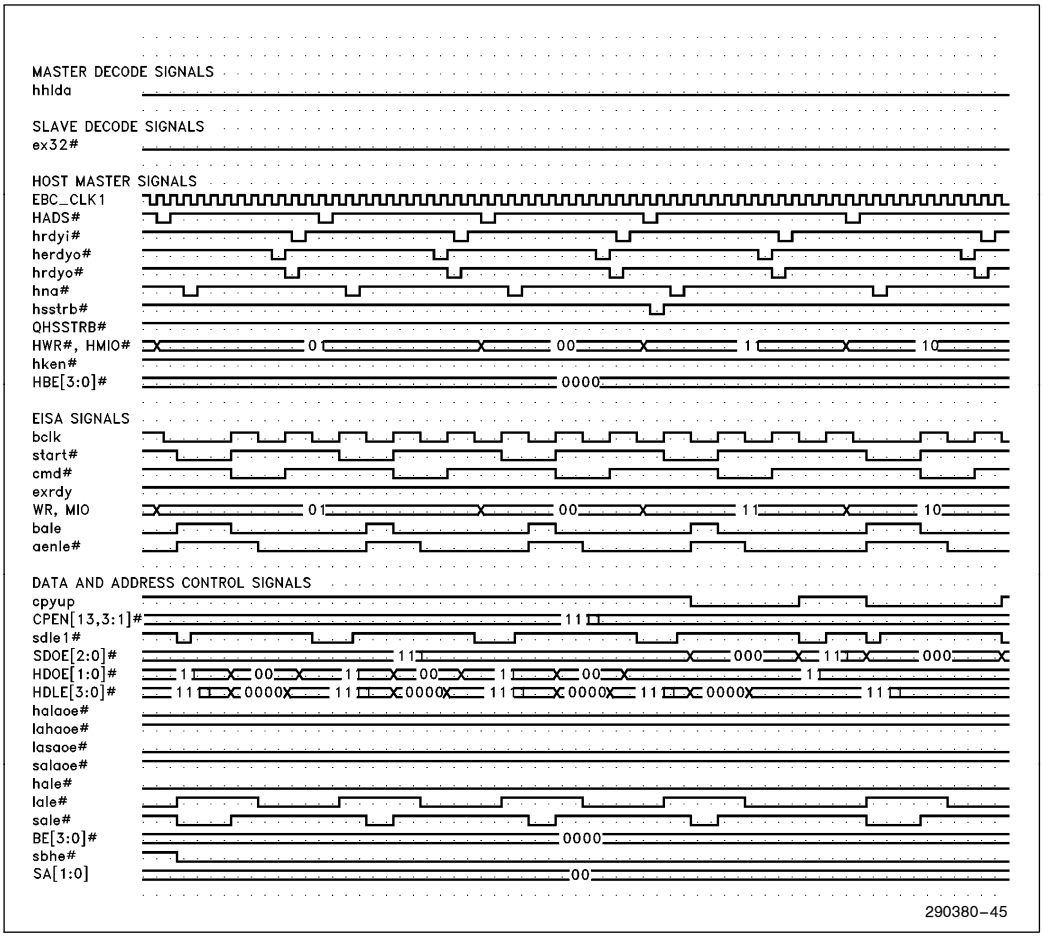


Figure 5-2. Host Master to 32-Bit EISA Slave Memory/IO Read, Memory/IO Write Standard Cycles-Four Byte Transfers

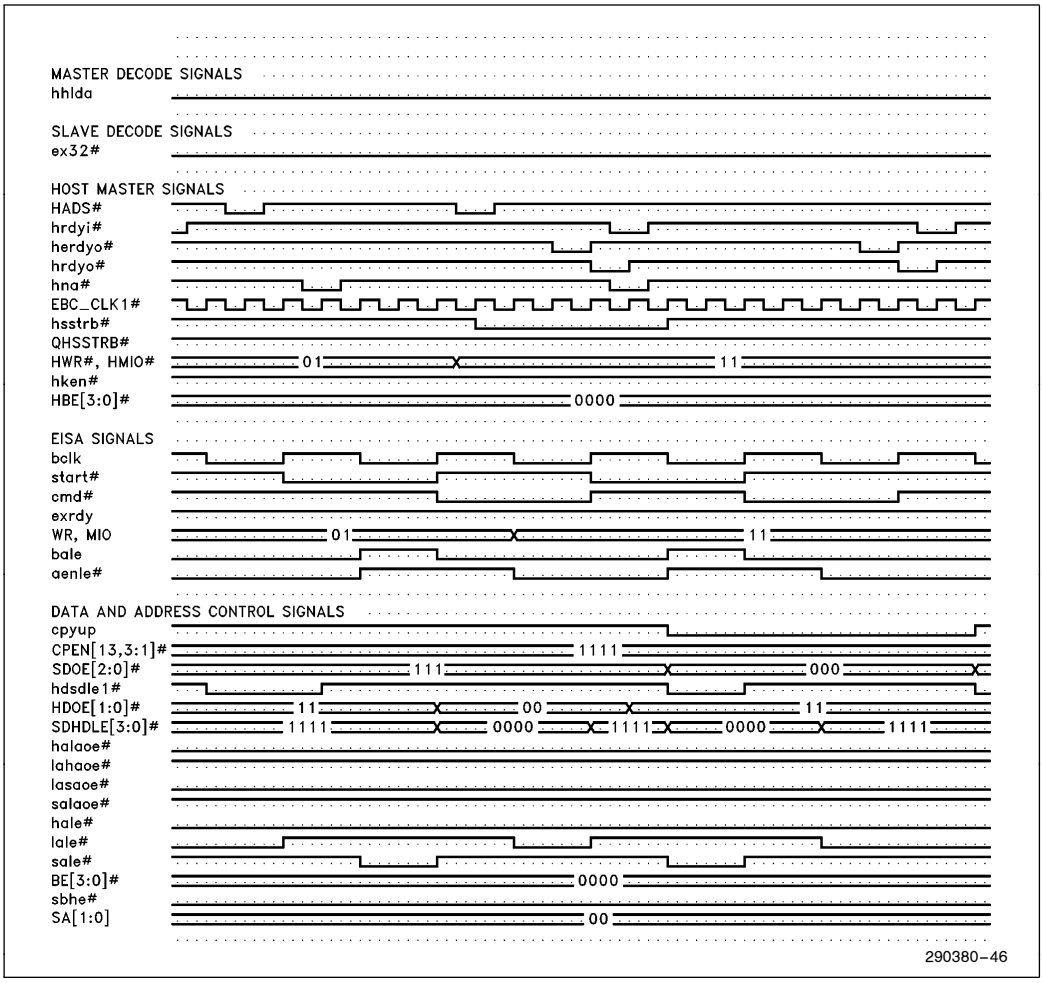


Figure 5-3. Host Master to 32-Bit EISA Memory Slave Standard Read Followed by a Pipelined Write Cycle-Four Byte Transfers

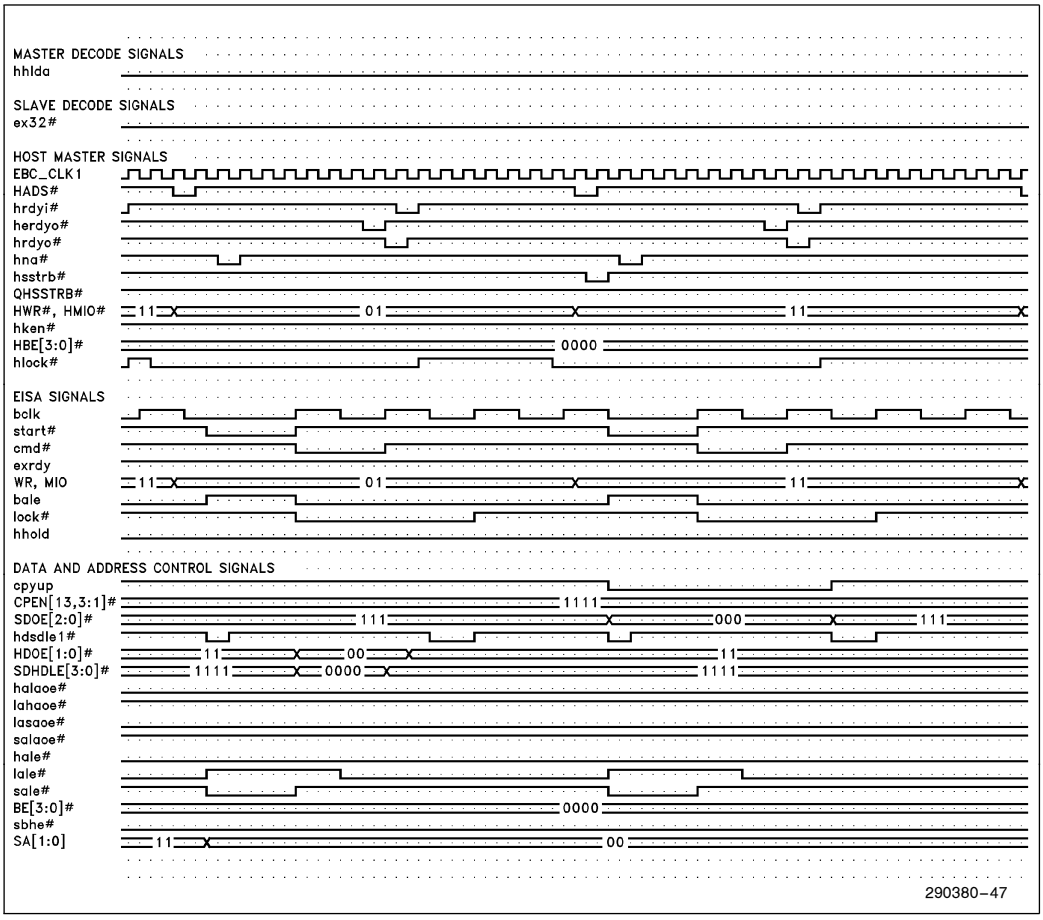


Figure 5-4. Host Master to 32-Bit EISA Memory Slave Locked Read Followed by a Locked Write Cycle-Four Byte Transfers

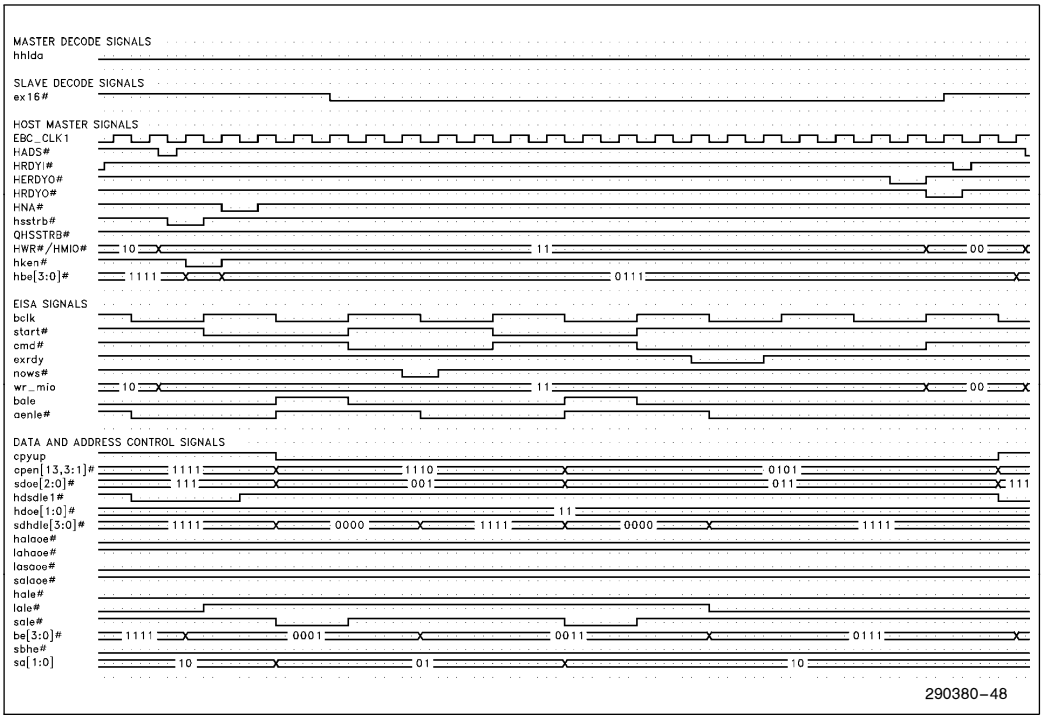


Figure 5-5. Host Master to 16-Bit EISA Memory Slave Disassembly Write Cycle-Three Byte Transfer

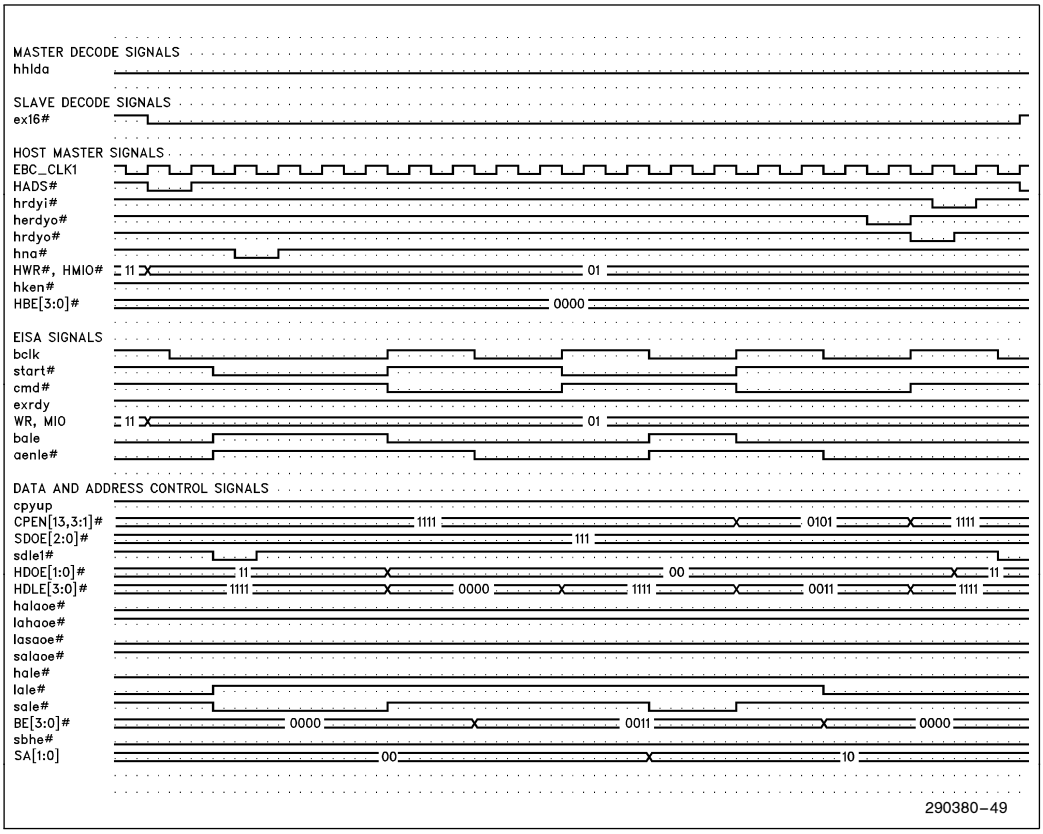


Figure 5-6. Host Master to 16-Bit EISA Memory Slave Assembly Read Cycle-Four Byte Transfer

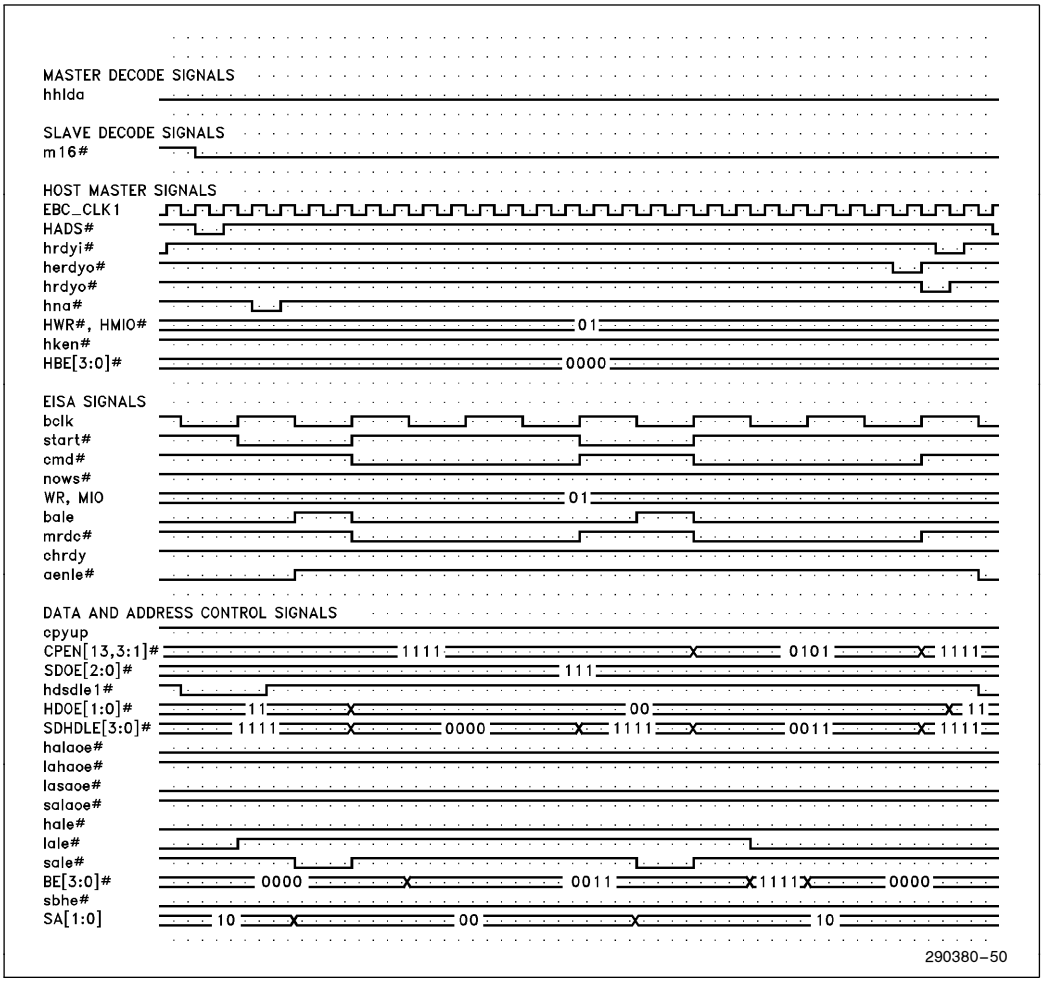


Figure 5-7. Host Master to 16-Bit ISA Memory Slave Assembly Read Cycle-Four Byte Transfer

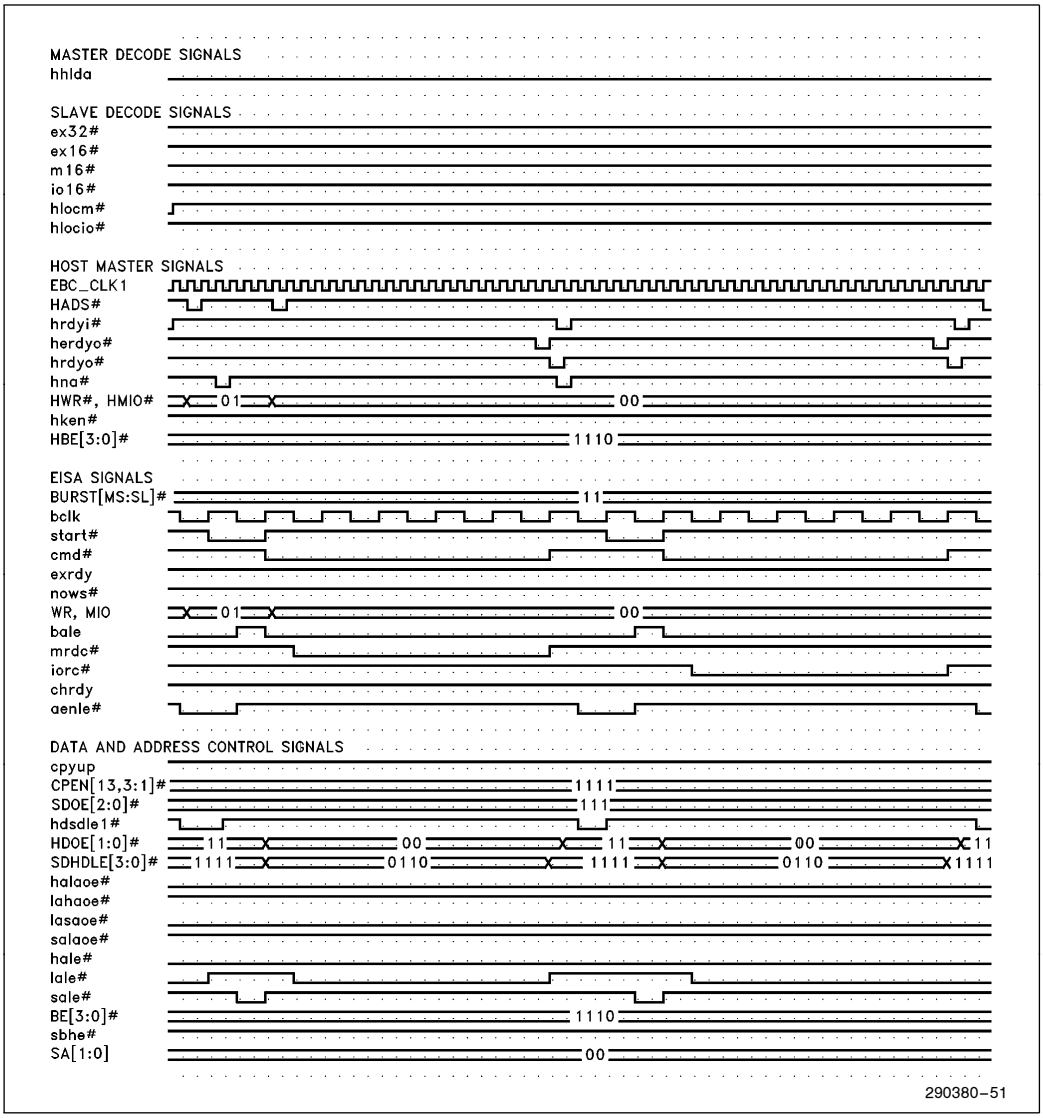


Figure 5-8. Host Master to 8-Bit ISA Slave, Memory Read Followed by a Pipelined I/O Read Cycle-One Byte Transfer

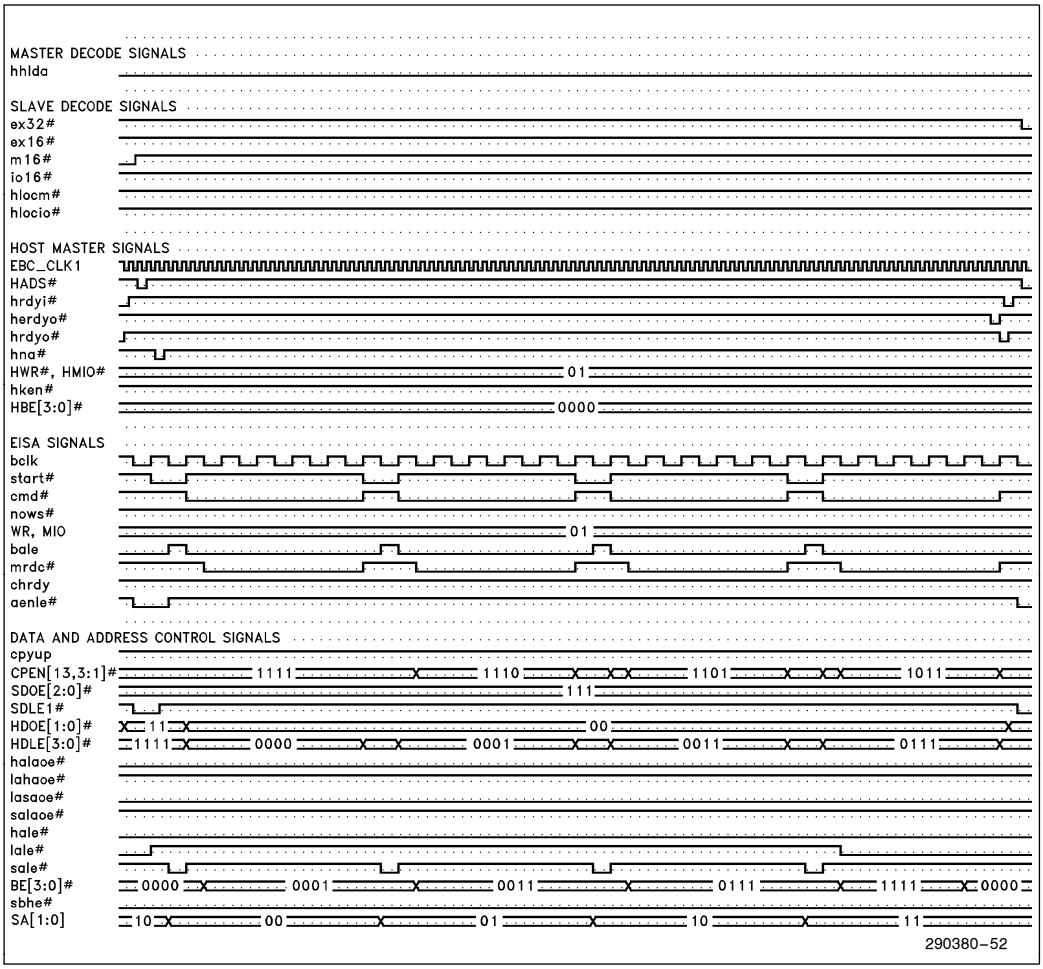


Figure 5-9. Host Master to 8-Bit ISA Memory Slave Assembly Read Cycle-Four Byte Transfer

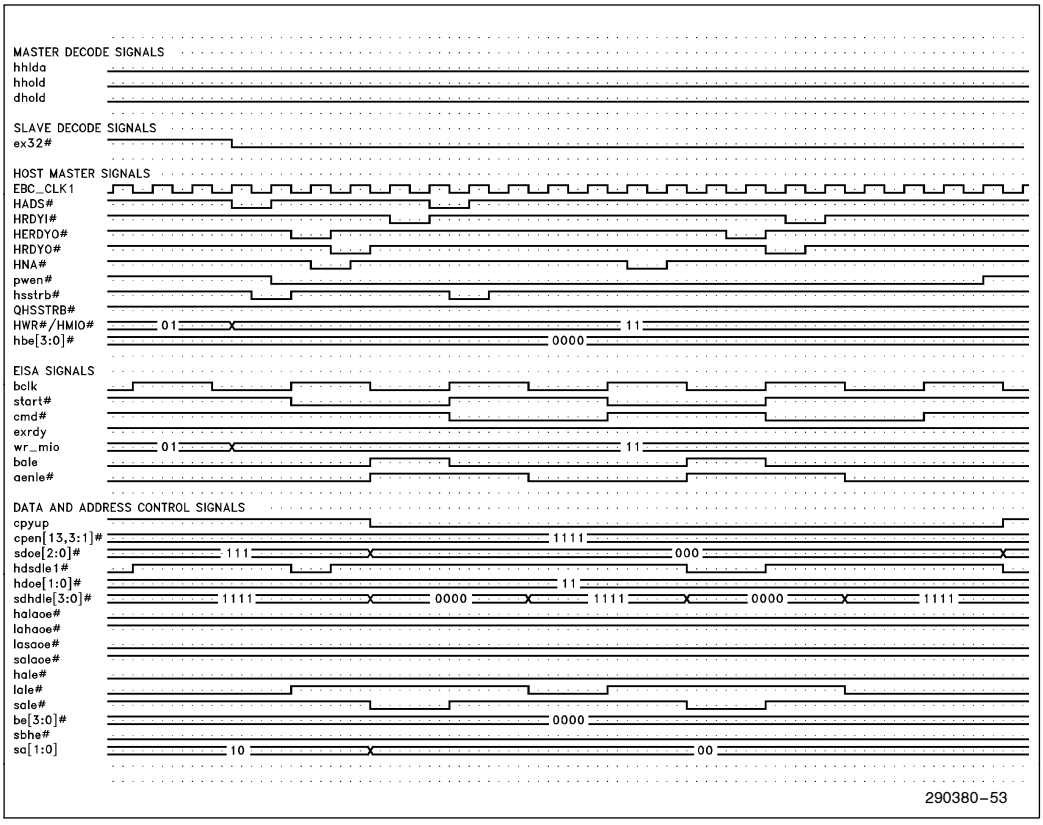


Figure 5-10. Host Master to 32-Bit EISA Slave Back-to-Back Posted Write Cycles-Four Byte Transfers

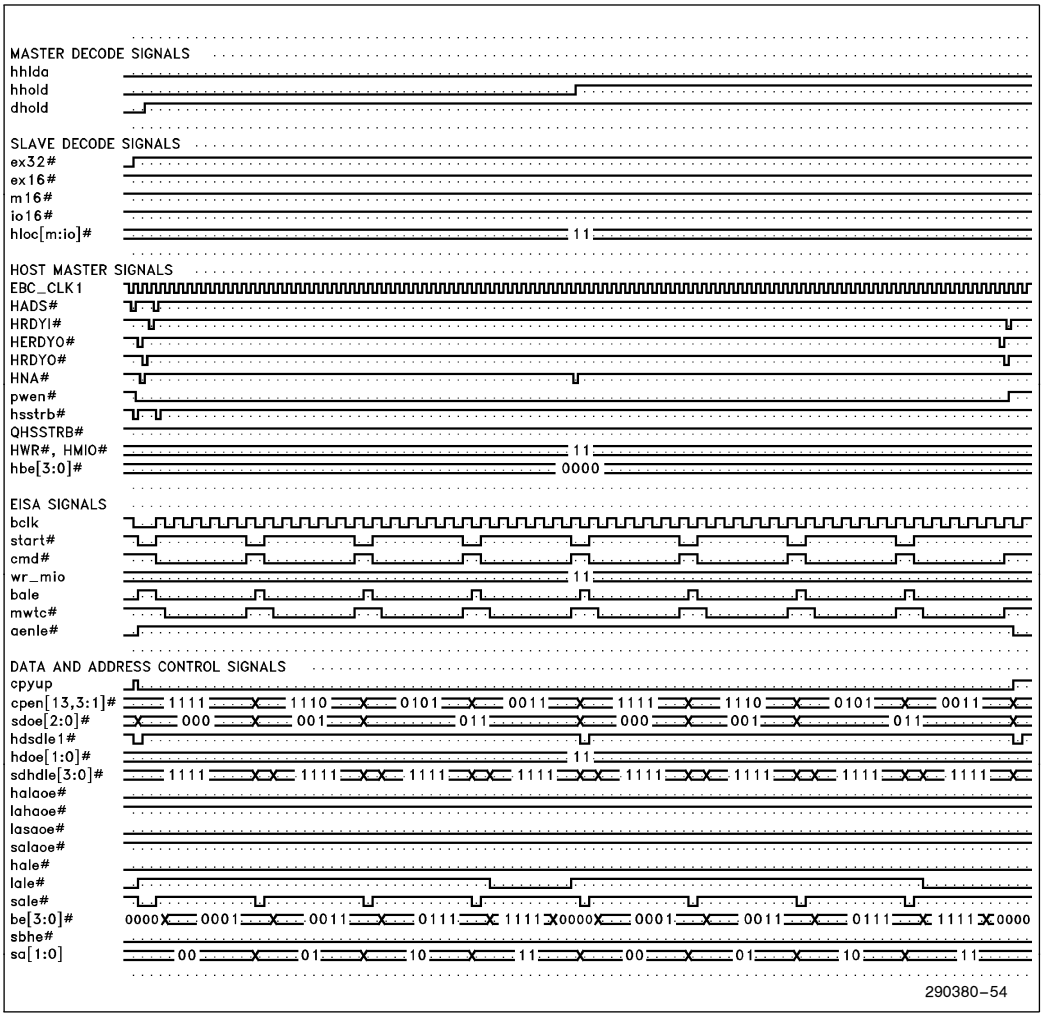


Figure 5-11. Host Master to 8-Bit ISA Memory Slave Posted Write Cycle with HHOLD Interlock-Four Byte Transfers

5.3 82350DT Host Master Cycles

If the EISA/ISA bus is not currently owned by a DMA, EISA, or ISA master, the host CPU has default access (i.e., access is automatic and it is not necessary to gain access through the system arbiter (ISP). However, if the bus is currently owned by a DMA, EISA, or ISA master, the host CPU must gain access to the EISA/ISA bus through the ISP. This is done via the ISP's CPUMISS# line.

[1]The beginning of an 82350DT host cycle starts with the 82359 DRAM controller driving AS# active, indicating that the address is valid on the EISA/ISA bus and HM/IO#, HW/R#, HD/C#, and HBE[3:0]# are valid on the host bus. The 82358DT then samples HLOCMEM# and HLOCIO# to determine if the host cycle needs to be forwarded to the EISA/ISA bus. [2]If the host master cycle is a memory cycle and HLOCMEM# is sampled inactive, or the host master cycle is an I/O cycle and HLOCIO# is sampled inactive, the 82358DT will drive ARDY low and generate the EISA/ISA command signals. [3]ARDY will remain inactive until the end of the cycle, indicating to the 82359 that the transfer is complete. The 82359 will then drive AS# inactive. The 82358DT provides all the data swap control if data size translation is necessary. The 82358DT determines if data size translation is necessary by sampling the slave and master decode signals at the start of the transfer (refer to section 4.3).

Any host cycle to the EISA/ISA bus can be extended by driving either EXRDY (EISA slave) or CHRDY (ISA slave) low. The number of wait states added depends on how long EXRDY or CHRDY are held low (refer to Table 4-6).

If a posted memory write cycle is indicated (PWEN# active), the 82358DT will terminate the cycle on the host bus by driving ARDY active after the host data has been latched on the rising edge of HDSDLE1#. The 82358DT will then complete the cycle on the EISA/ISA bus. Refer to section 4.1.3 for additional information regarding posting of memory writes.

NOTES:

(1) **In an 82350DT/enhanced configuration**, the 82358DT controls the propagation of the HA[31:2] address through the address buffers onto the SA[19:2] and ISP address buses. The 82358DT also translates the HBE[3:0]# lines to SA0, SA1, SBHE#, and BE[3:0]#. The LA[31:2] address, W-R, and M-IO signals are tied directly to the 82359 DRAM controller, bypassing the address buffers.

In an 82350DT/buffered configuration, the 82358DT controls the propagation of the HA[31:2] address through the address buffers, onto the LA[31:2] and SA[19:2] buses. The 82358DT also translates the HBE[3:0]# lines to SA0, SA1, SBHE#, and BE[3:0]#, and HW/R# signal to W-R. HM/IO# is propagated to the EISA bus along with address lines.

(2) If the cycle is directed at an EISA slave, only the EISA command signals will be generated (START# and CMD#). If the cycle is directed at an ISA slave, both the EISA command signals and the ISA command signals (IORC#, IOWC#, MRDC#, or MWTC#, depending on the slave type) will be generated. Please refer to Table 4-9.

(3) ARDY will remain inactive until the transfer is complete, except in the following cases: For posted memory write cycles and the first cycle of an i486 burst read, ARDY is driven active prior to the completion of the cycle on the EISA/ISA bus. For subsequent i486 burst read cycles, the last rising edge of SDVLD is used to indicate to 82359 DRAM controller that the transfer is complete. SDVLD is also used by the 82353 (ADP) to indicate that valid read data is setup to its internal latches and can be frozen.

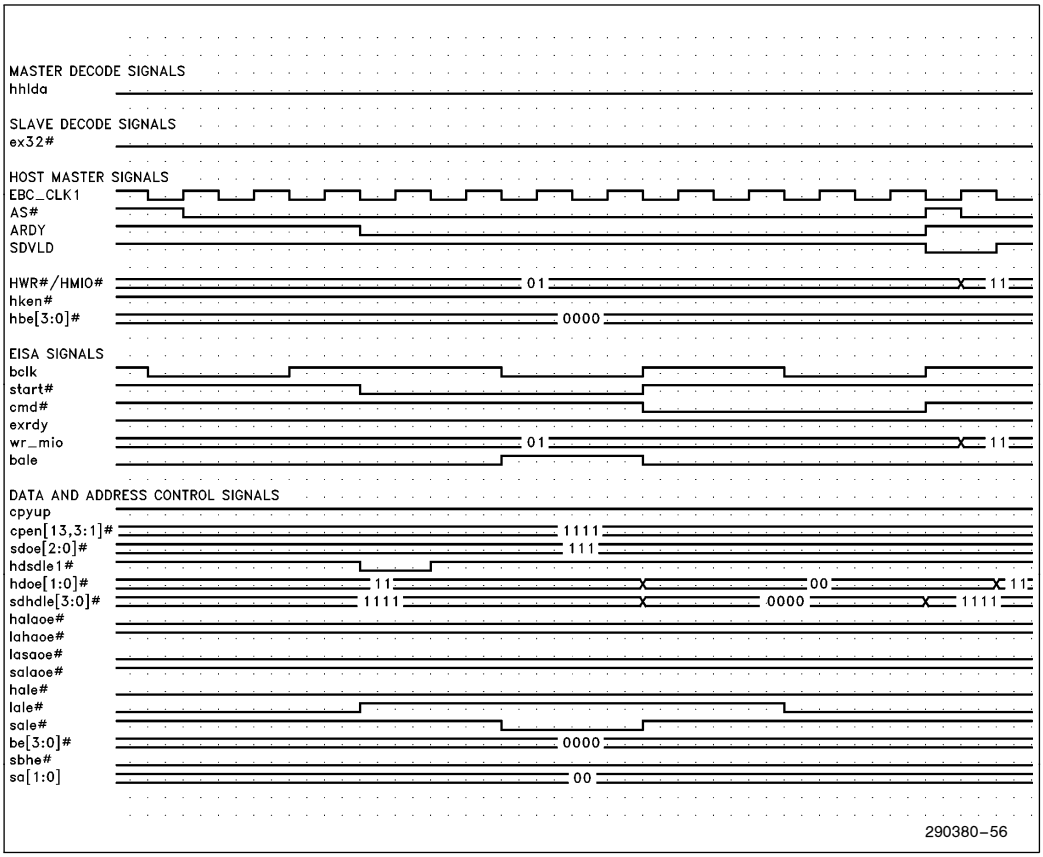


Figure 5-12. Host Master to 32-Bit EISA Memory Slave Standard Read Cycle-Four Byte Transfer

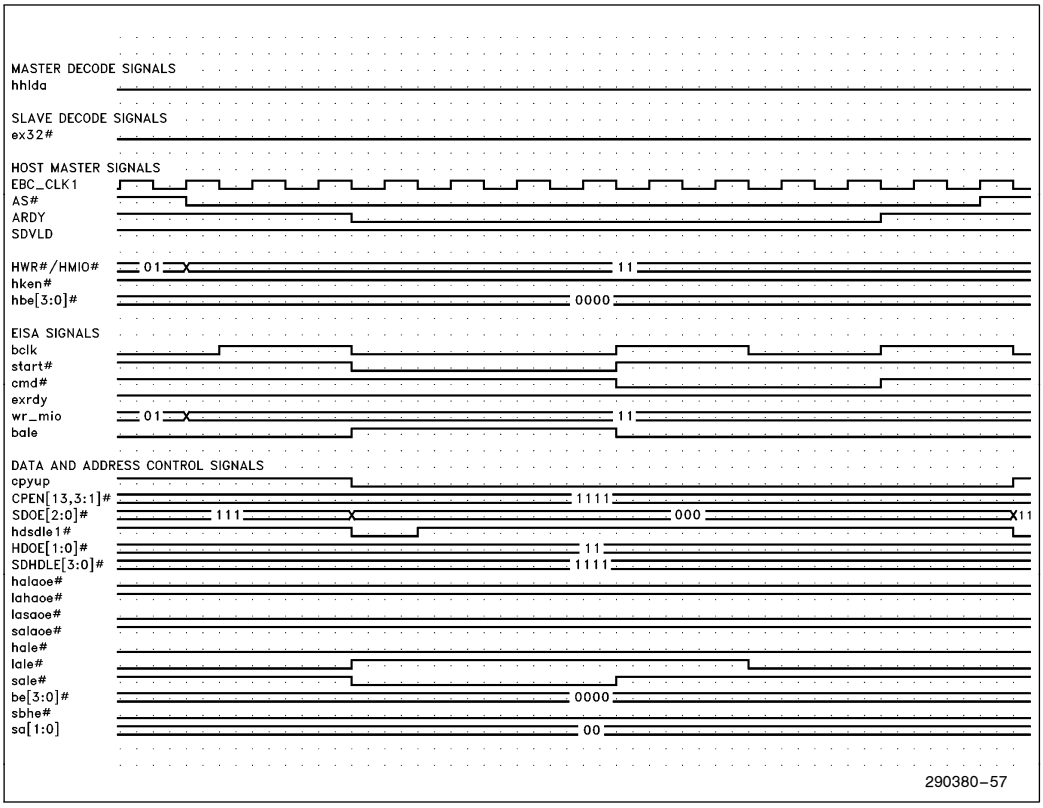


Figure 5-13. Host Master to 32-Bit EISA Memory Slave Standard Write Cycle-Four Byte Transfer

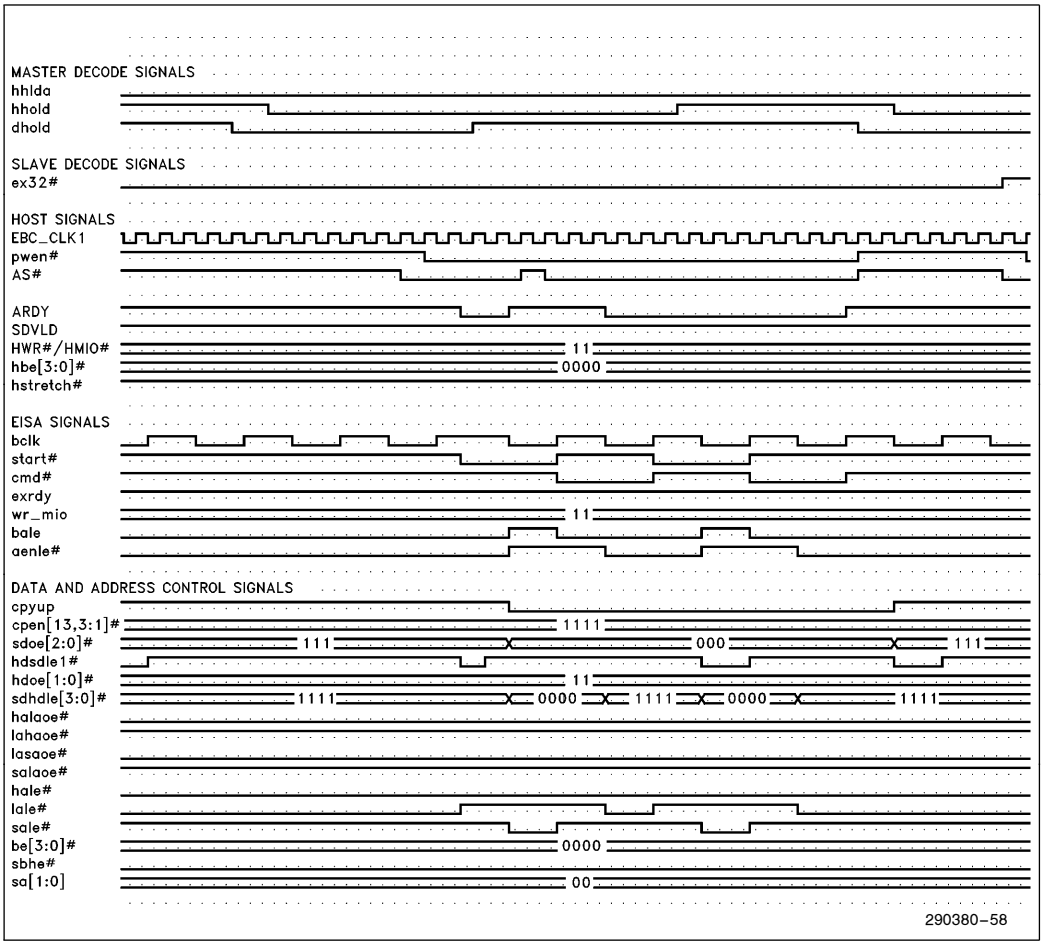


Figure 5-14. Host Master to 32-Bit EISA Memory Slave Posted Write Cycles with HHOLD Interlock-Four Byte Transfers

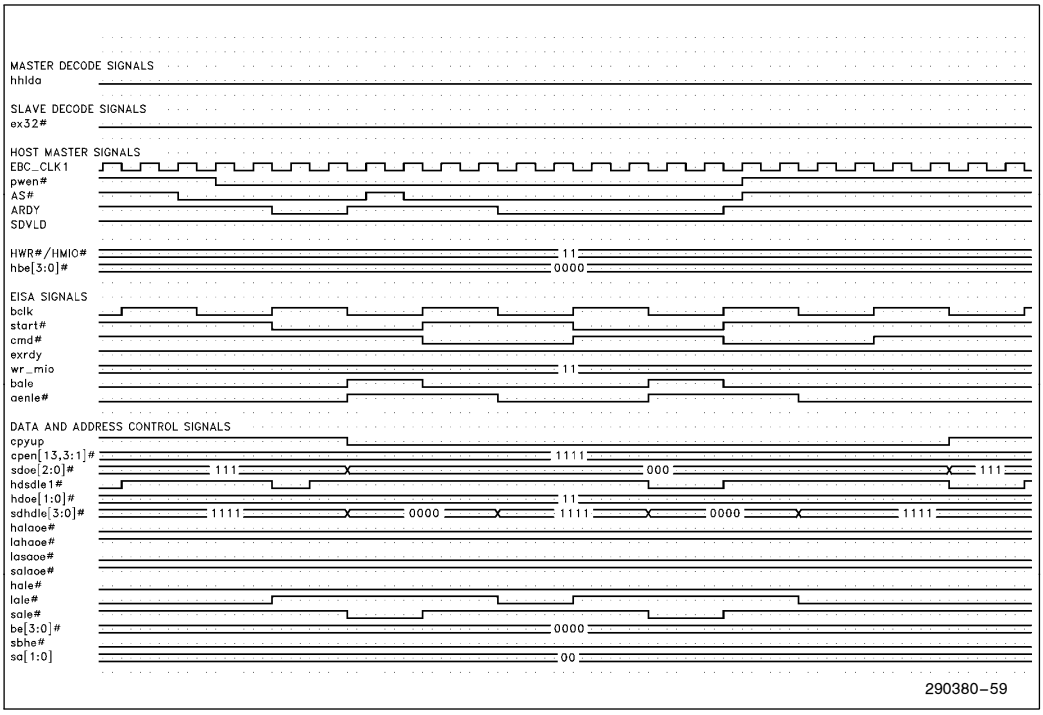


Figure 5-15. Host Master to 32-Bit EISA Memory Slave Back-to-Back Posted Write Cycle-Four Byte Transfers

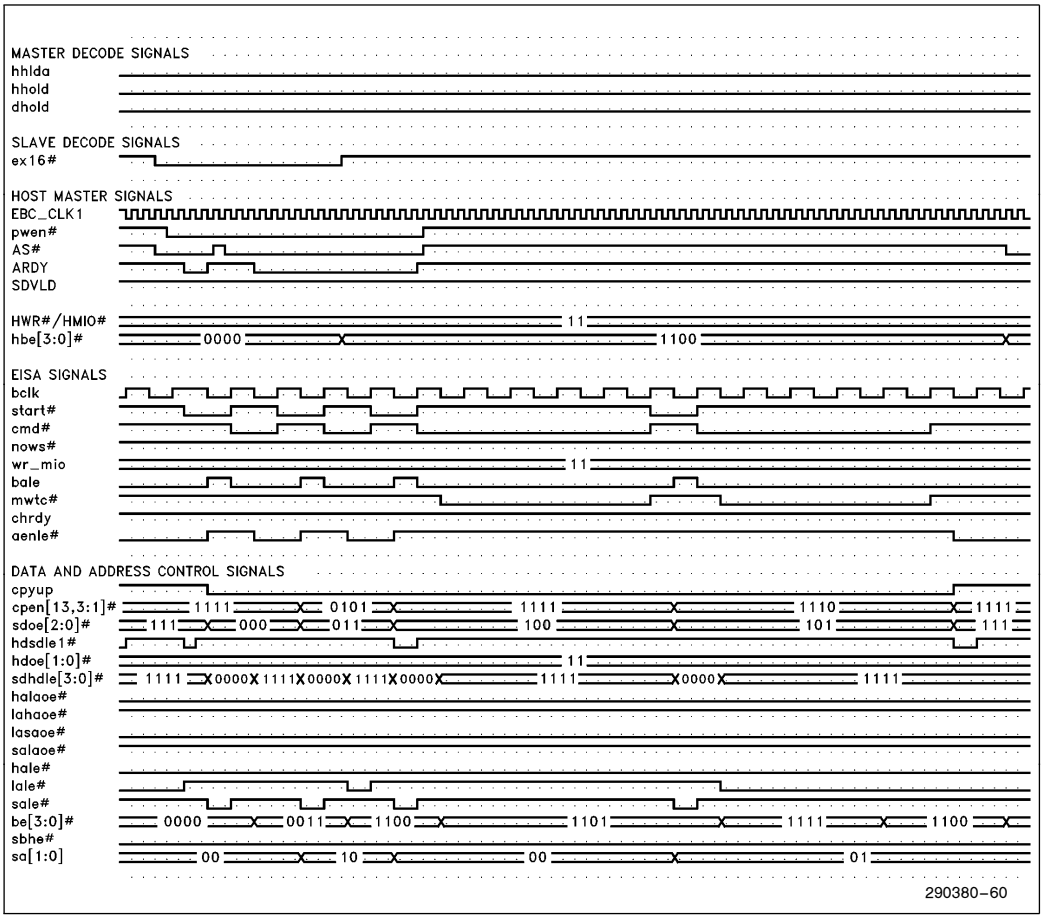


Figure 5-16. Host Master to 16-Bit EISA and 8-Bit EISA/ISA Slave Back-to-Back Posted Memory Write Cycle-Four Byte Followed by a Two-Byte Transfer

5.4 EISA Master Cycles

The EISA master gains control of the bus by asserting its master request line (MREQx) to the system arbiter (82357/ISP). After sampling the EISA masters MREQx line active, the ISP, if the bus is currently available and the EISA master has highest priority, drives the EISA masters corresponding master acknowledge (MACKx) signal active. The EISA master then starts the cycle on the EISA bus by driving the address, M-IO, and W-R signals.

[1]The beginning of a cycle starts with the EISA bus master driving a valid address onto the LA[31:2] bus and asserting BE[3:0]#, M-IO, and W-R, indicating the cycle type (memory or I/O, read or write). [2]The 82358DT controls the propagation of the LA[31:2] address through the address buffers onto the HA[31:2] and SA[19:2] buses, translates the BE[3:0]# lines to SA0, SA1, SBHE#, and HBE[3:0]#, and translates W-R to HW/R#. At this time, the EISA master may also assert MASTER16# if it is a 16-Bit EISA master.

[3]After decoding the address as its own, the memory or I/O slave asserts the appropriate signals to indicate the type of slave and whether or not it can perform any special timings (e.g., Burst).

The EISA master then asserts START# to indicate the start of the current cycle. The 82358DT samples the slave decode signals (HLOCMEM#, HLOCIO#, EX16#, EX32#, M16#, and IO16#) at the end of START# to determine the slave size and type. [4]The 82358DT uses this information to determine if ISA cycles need to be generated and whether data size translation is necessary.

The 82358DT asserts CMD# simultaneously with the negation of START# to control the data transfer to or from the slave. The master may also assert MSBURST# at this time if the master supports bursting and the slave has driven SLBURST# active. CMD# will remain active until the end of the cycle. If the slave device is an ISA device, the 82358DT will also assert one of the ISA command signals (IORC#, IOWC#, MRDC#, or MWTC#) during CMD#, depending on the slave type.

For EISA/ISA read cycles, the read data is setup and held to the same rising edge of BCLK that CMD# is negated. For EISA/ISA write cycles and the first cycle of a EISA burst write cycle, the master drives the write data valid prior to the falling edge of CMD# and holds it until the falling edge of BCLK after CMD# is negated. For EISA burst read cycles, the read data is setup and held to every rising edge of BCLK after the rising edge of BCLK that START# is negated until the burst cycle is complete (MSBURST# negated). For subsequent EISA write burst cycles, the master drives the valid data from the rising edge of BCLK after START# is negated and holds it valid until the next rising edge of BCLK, continuing this process from clock to clock until the burst is complete (MSBURST# negated).

Wait states can be added by the slave device either by negating EXRDY (EISA/host slaves) or CHRDY (ISA slaves). The 82358DT samples both EXRDY and CHRDY during EISA master cycles and will lengthen the cycle by holding CMD# and/or the ISA command signals active until after EXRDY and CHRDY are sampled active. A host slave cycle may also be extended by driving HSTRETCH# low. The cycle will be extended until HSTRETCH# is driven inactive (refer to section 4.9).

NOTES:

(1) For EISA non-burst cycles and the first cycle of a burst, the EISA master holds the address, BE[3:0]#, and cycle definition signals active until the falling edge of BCLK after CMD# is asserted. For subsequent burst transfers, the address signals change on every falling edge of BCLK after START# is negated, until the end of the burst. If wait states are added (EXRDY negated), the address signals will not change until EXRDY is negated.

(2) In the case of an 82350DT/enhanced configuration, the LA address lines, M-IO, and W-R lines are tied directly to the 82359 (refer to section 4.1.2.2).

(3) An EISA slave will assert either EX16# (indicating 16-bit EISA memory or I/O), or EX32# (indicating 32-bit EISA memory or I/O), depending on its data bus size. The EISA memory slave will also assert SLBURST# if it is capable of supporting EISA burst cycles. If the slave device is 8-bits, neither EX16# nor EX32# will be asserted.

An ISA slave will assert either M16# (indicating 16-bit ISA memory), or IO16# (indicating 16-bit I/O). The ISA slave will also assert NOWS# if no wait state cycles are supported. If the slave device is 8-bits, neither M16# nor IO16# will be asserted.

A host slave will assert either HLOCMEM# (indicating 32-bit host memory), or HLOCIO# (indicating 32-bit host I/O). In either case, the 82358DT will assert EX32# indicating to the EISA master that the host slave is 32-bits and can support EISA cycles.

Refer to section 4.3 for additional information regarding slave/master decode.

(4) If data size translation is required, the master must back-off the bus by floating its data lines, BE[3:0]# lines, and START# signal to allow the 82358DT to generate any subcycles that may need to be generated (refer to section 4.5). At the end of the transfer, the 82358DT gives cycle control back to the master by asserting EX16# and EX32#, indicating to the master that it now has control of the cycle and that cycle translation is complete.

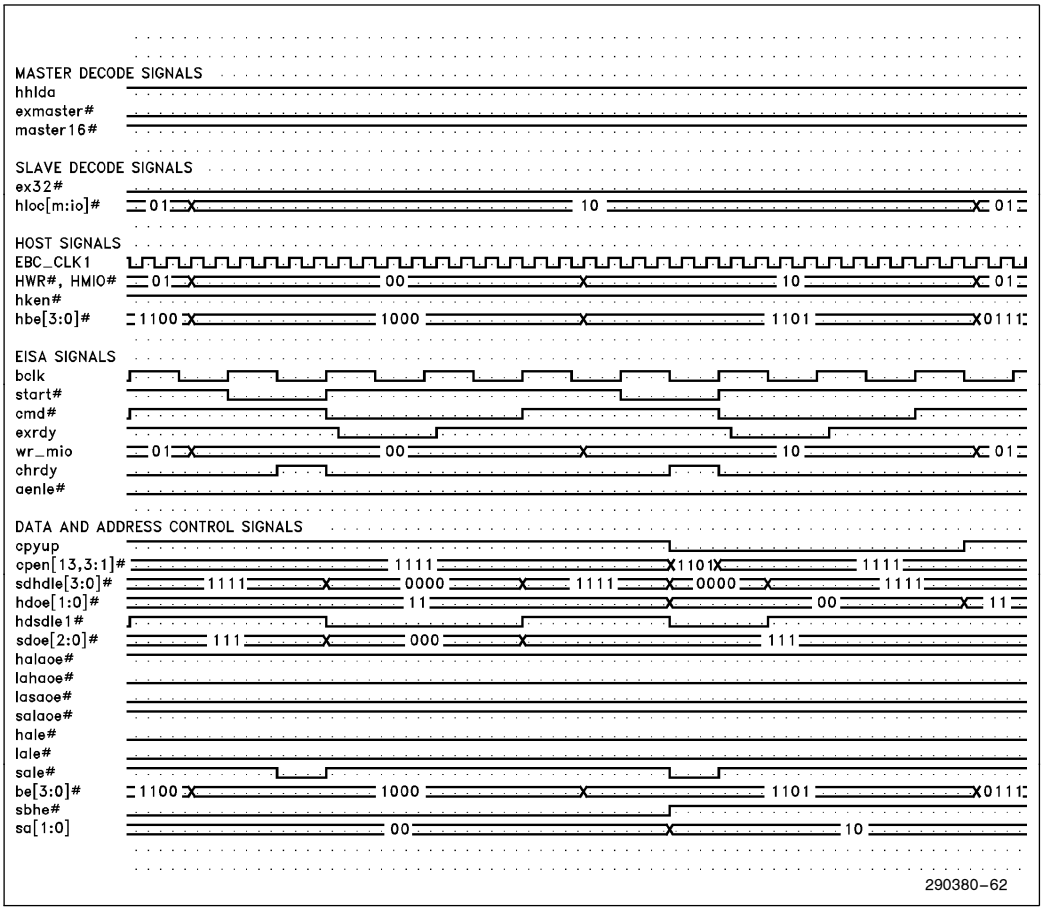


Figure 5-17. 32-Bit EISA Master to Host I/O Slave Read Followed by a Write Cycle with One Wait State-Three Byte Followed by One Byte Transfer

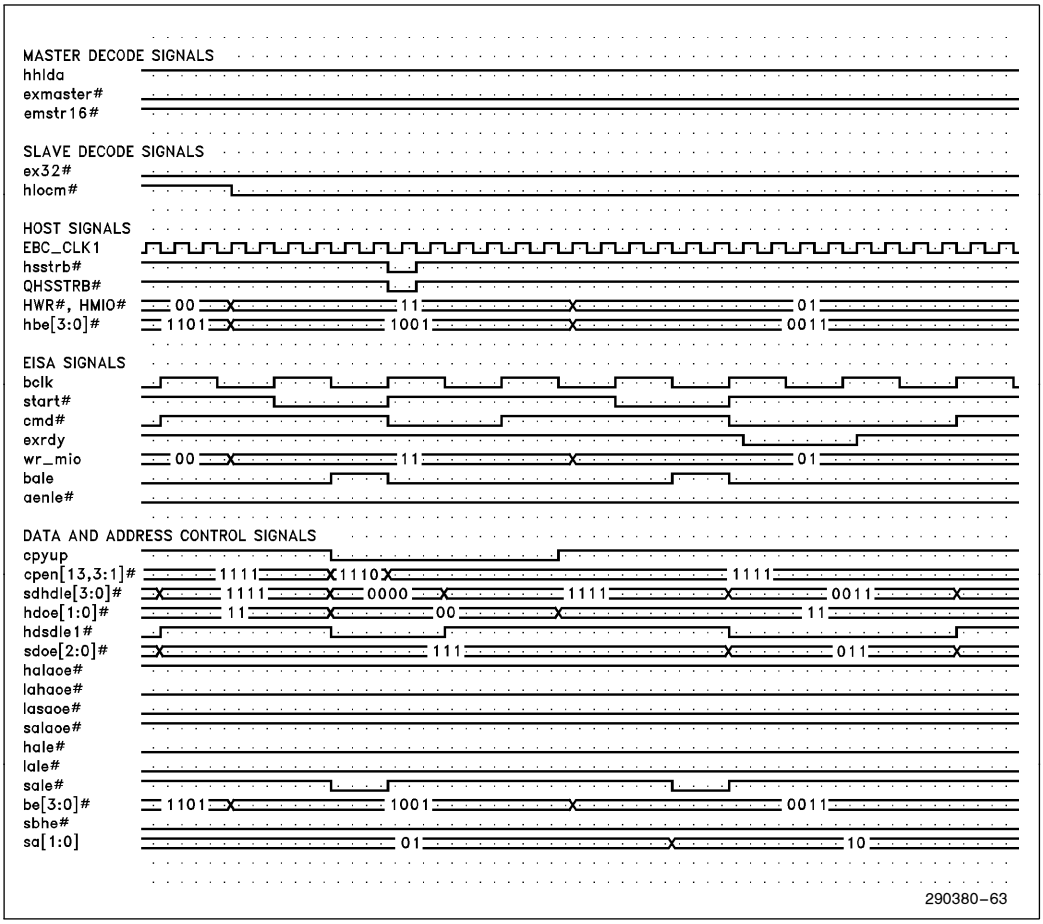


Figure 5-18. 32-Bit EISA Master to Host Memory Slave Write Followed by a Read Cycle with One Wait State-Two Byte Transfers

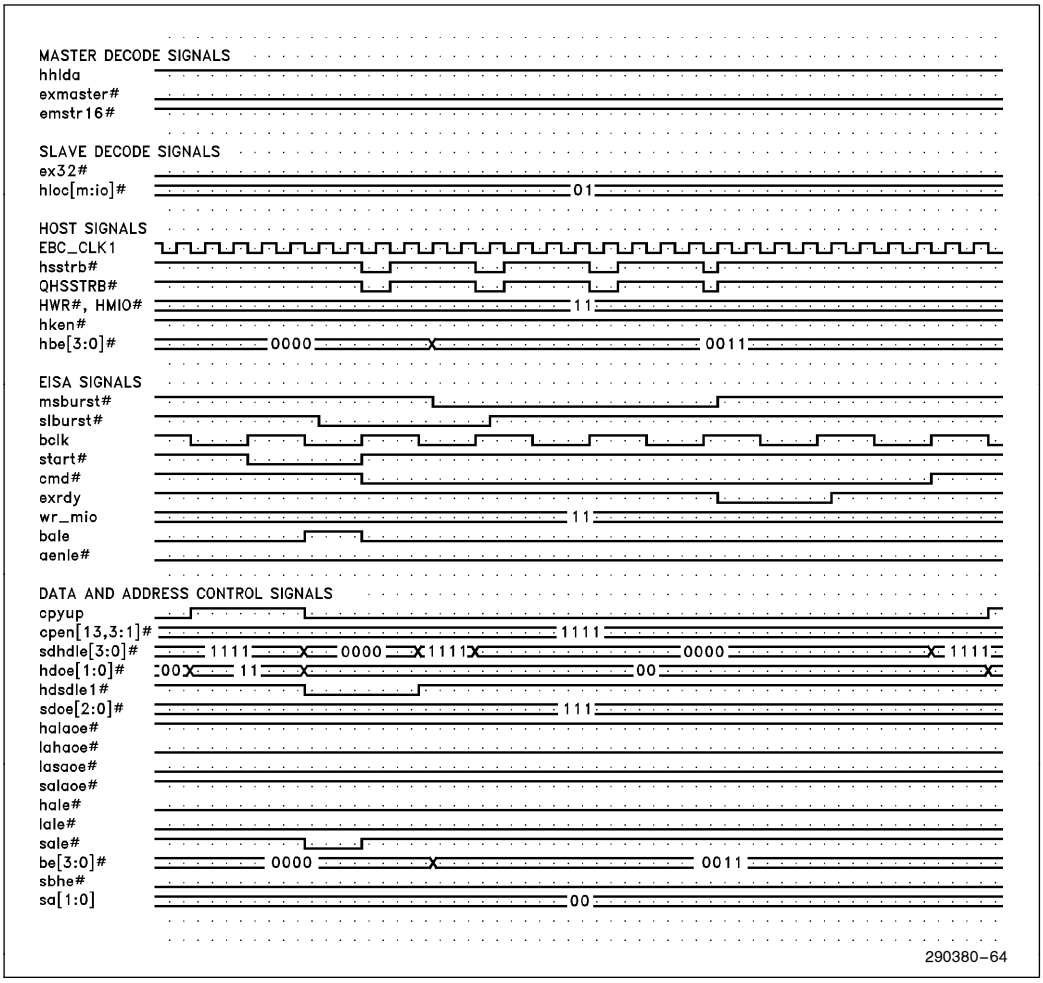


Figure 5-19. 32-Bit EISA Master to Host Memory Slave Burst Write Cycle with One Wait State

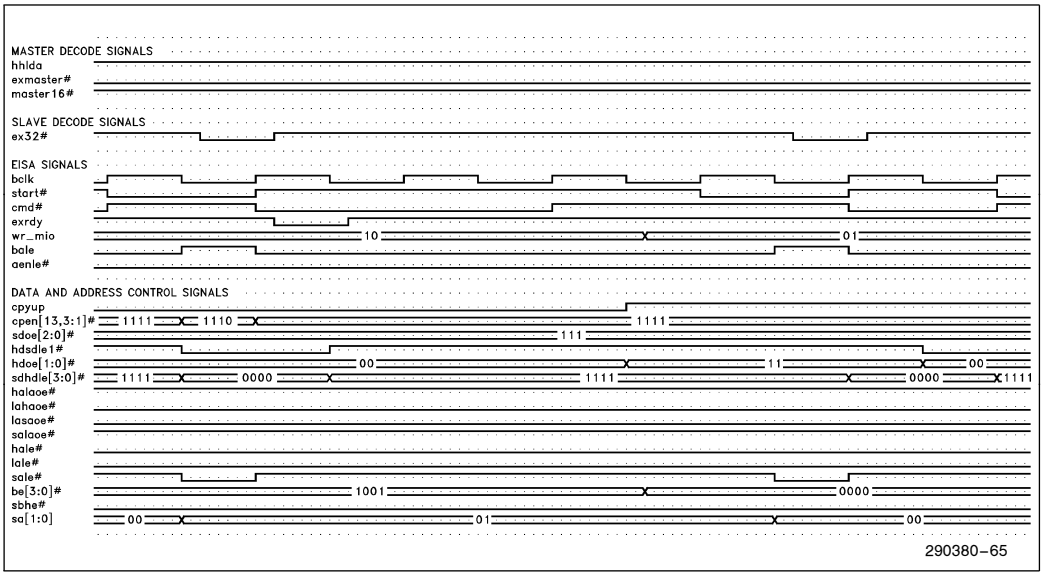


Figure 5-20. 32-Bit EISA Master to 32-Bit EISA Slave I/O Write with One Wait State Followed by a Memory Read Cycle-Two Byte and Four Byte Transfers

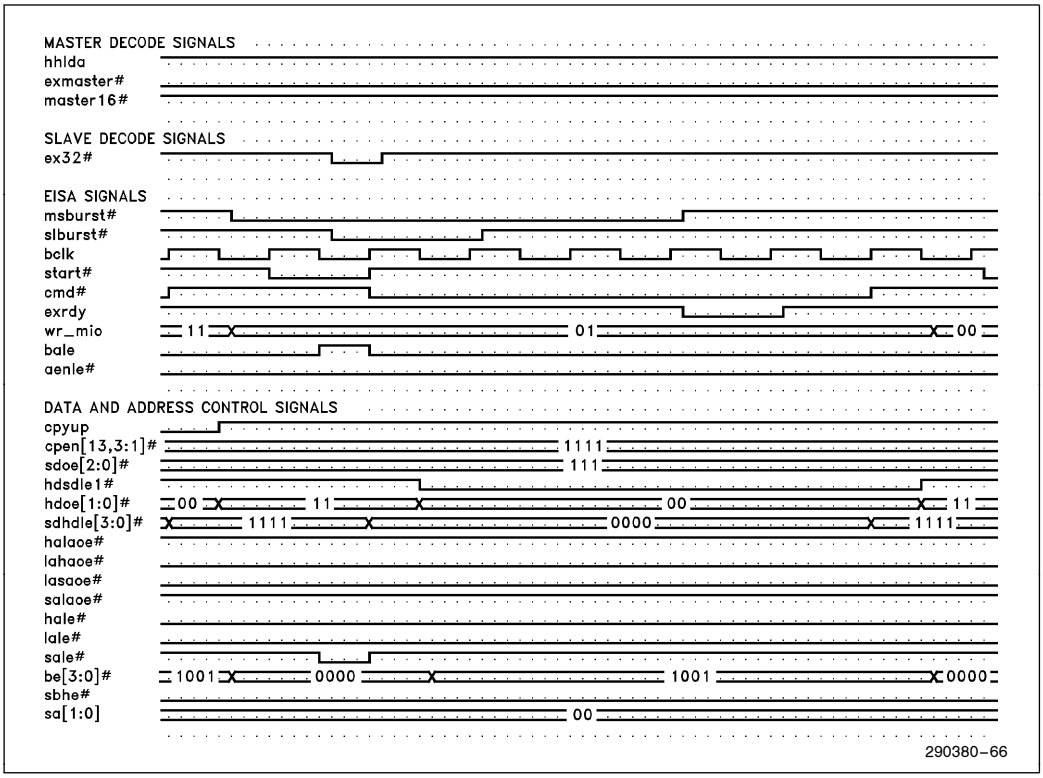


Figure 5-21. 32-Bit EISA Master to 32-Bit EISA Memory Slave Burst Read Cycle with One Wait State

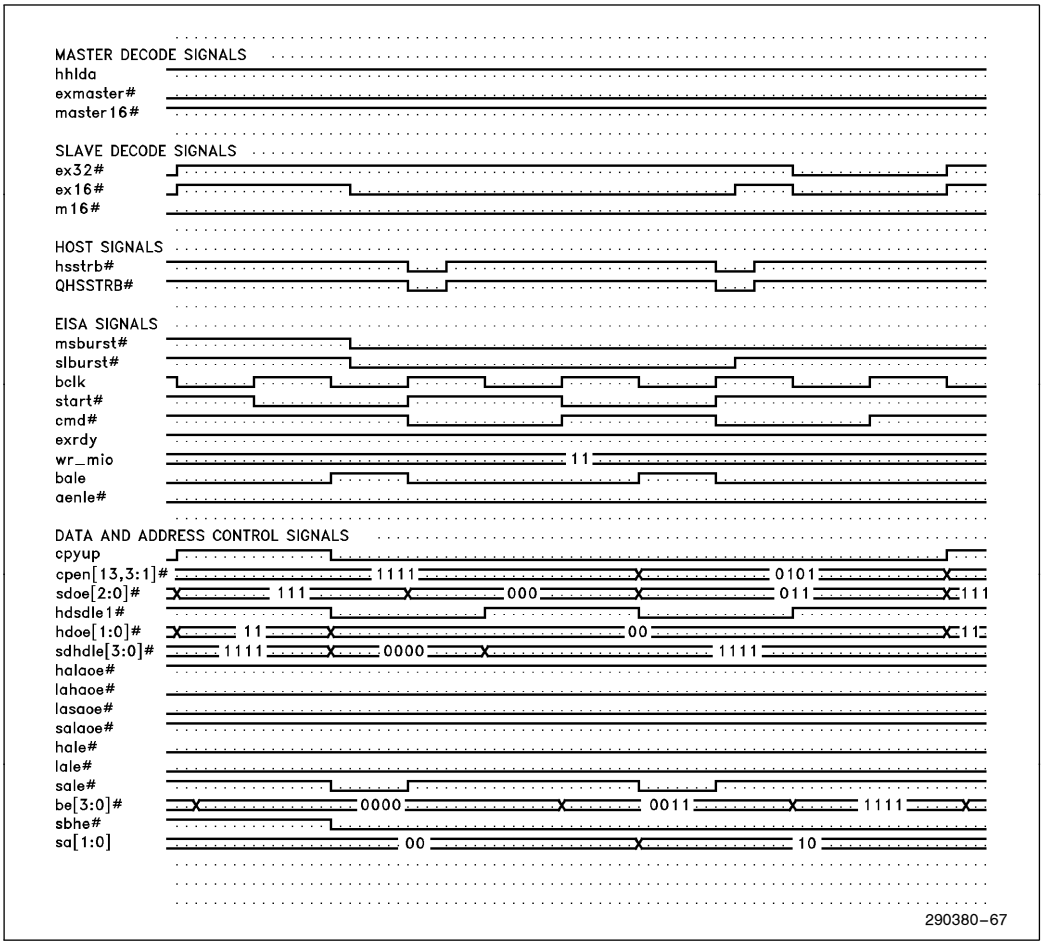


Figure 5-22. 32-Bit EISA Master to 16-Bit EISA Memory Slave Burst Back-Off Write Disassembly Cycle-Four Byte Transfer

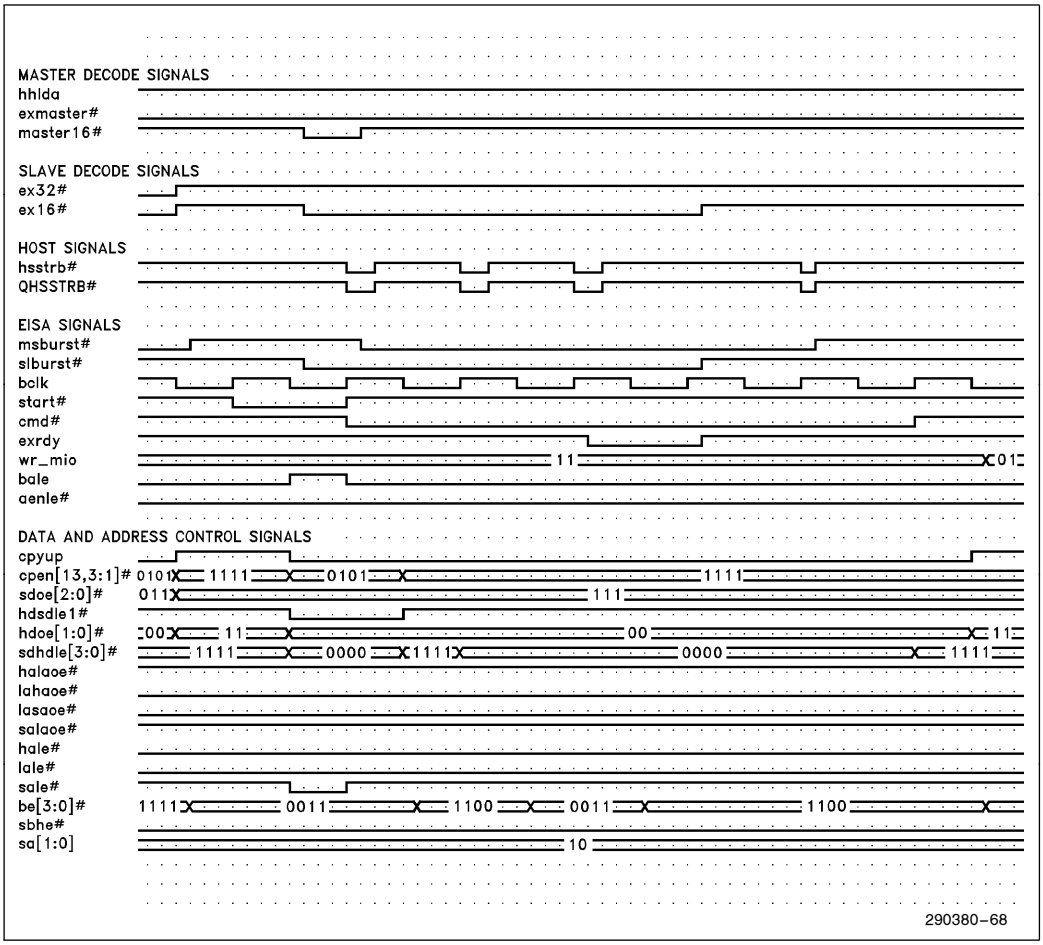


Figure 5-23. 32-Bit EISA Master to 16-Bit EISA Memory Slave Downshift Burst Write Cycle

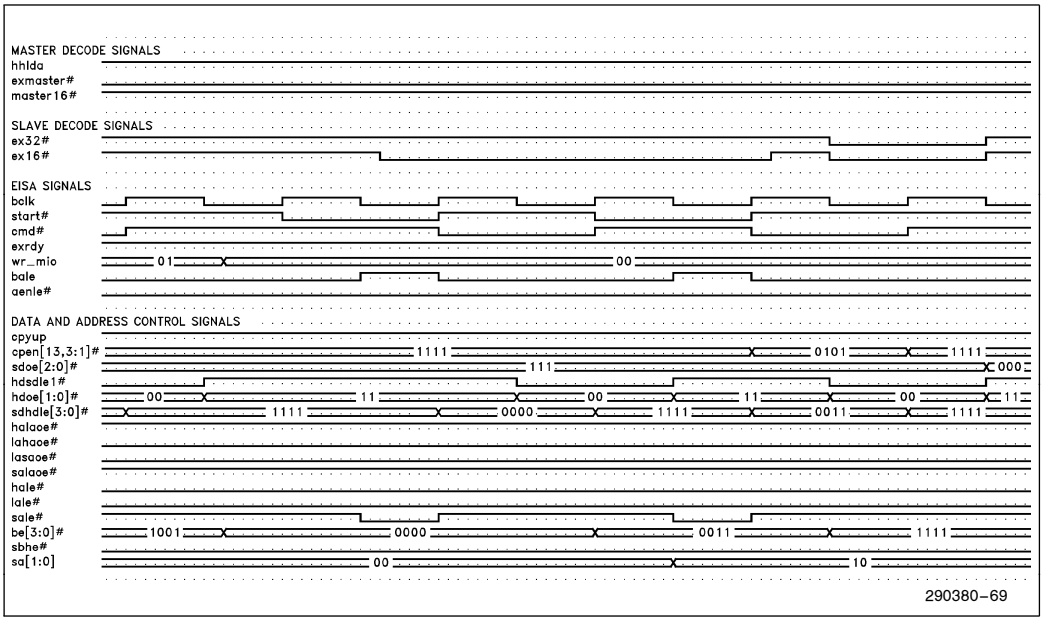


Figure 5-24. 32-Bit EISA to 16-Bit EISA I/O Read Assembly Cycle-Four Byte Transfer

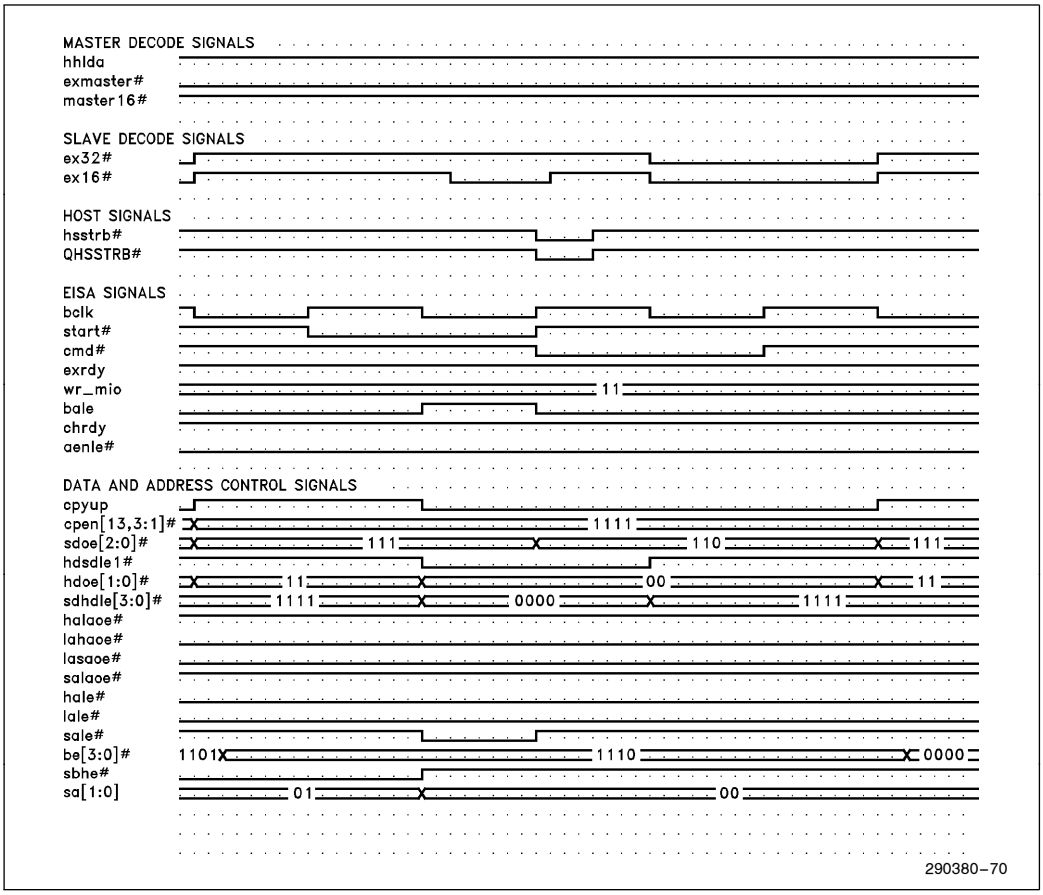


Figure 5-25. 32-Bit EISA Master to 16-Bit EISA Memory Slave Standard Write Cycle-One Byte Transfer

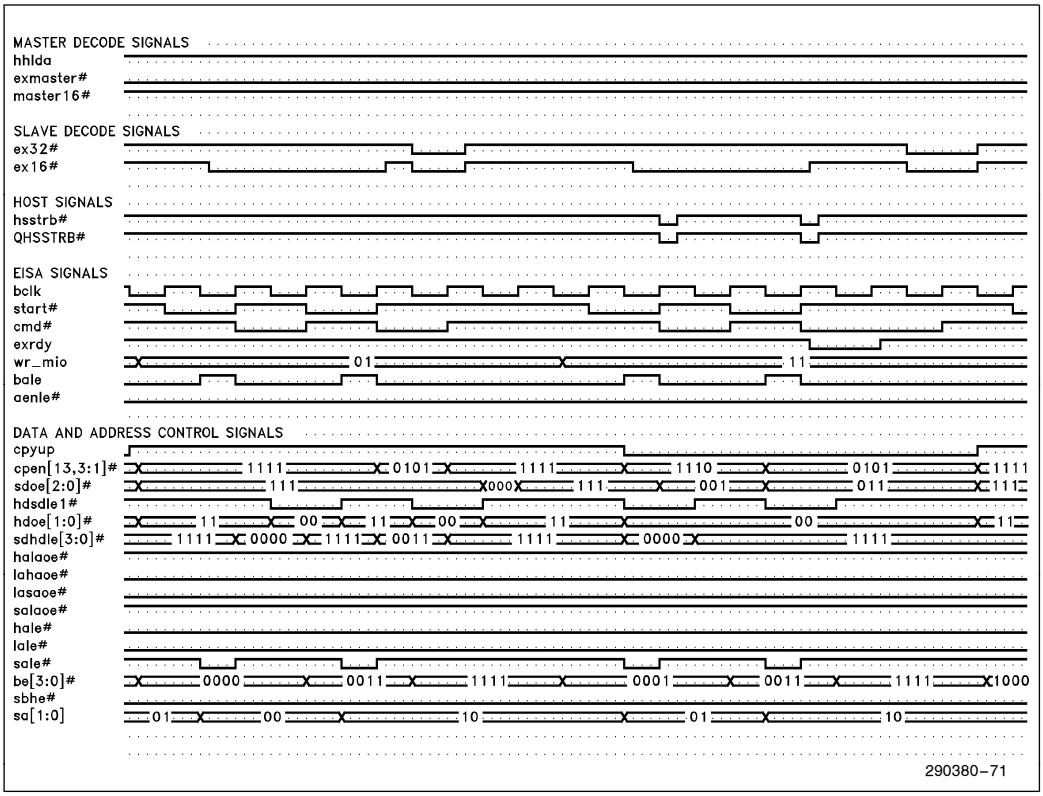


Figure 5-26. 32-Bit EISA Master to 16-Bit EISA Memory Slave Assembly Read Followed by a Disassembly Write Cycle with One Wait State-Four Byte Followed by Three Byte Transfer

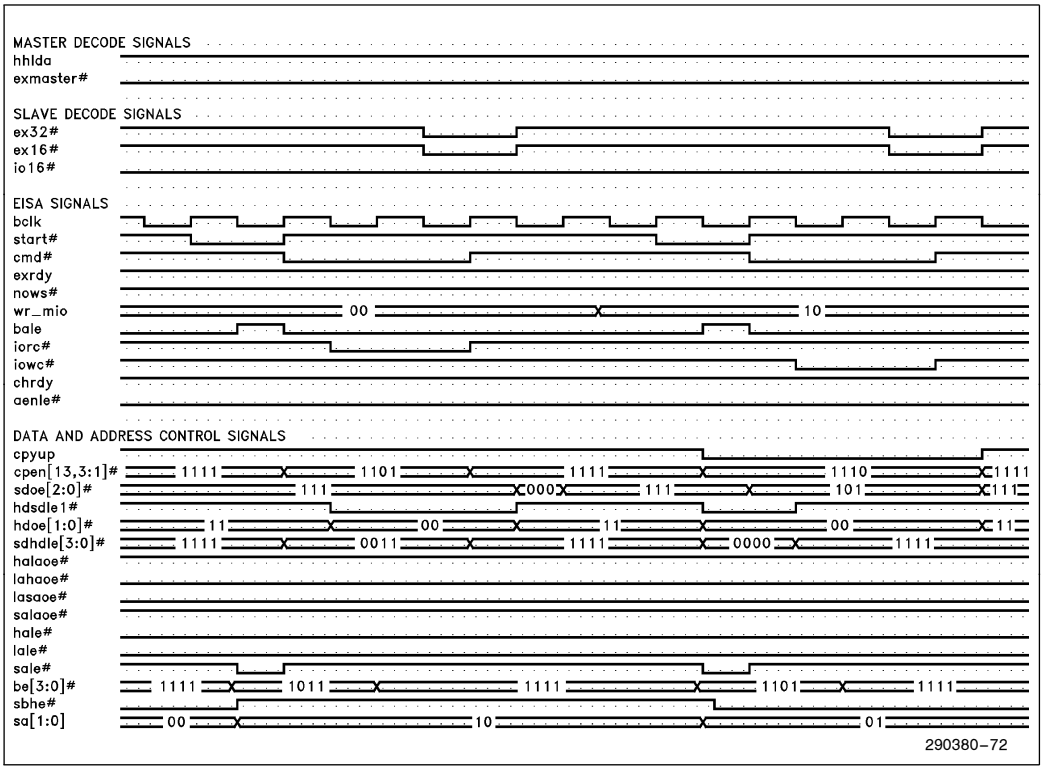


Figure 5-27. 32-Bit EISA Master to 16-Bit ISA I/O Slave Standard Read Followed by a Write Cycle-One Byte Transfers

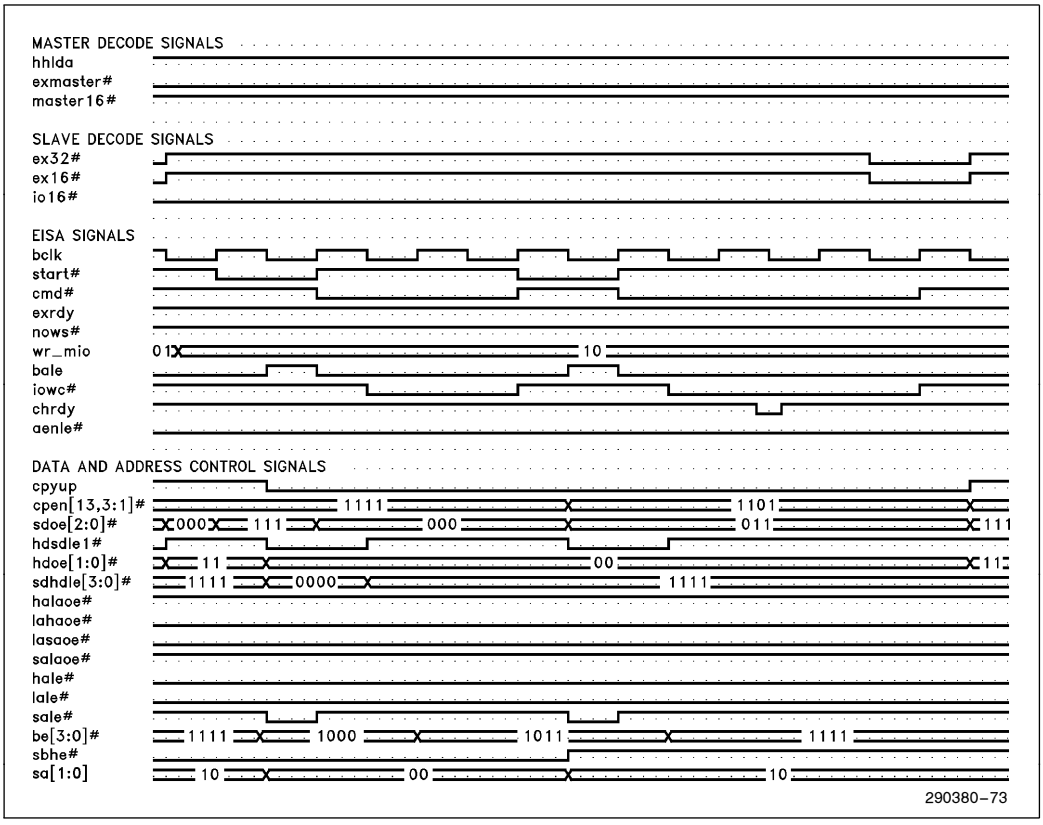


Figure 5-28. 32-Bit EISA Master to 16-Bit ISA I/O Slave Write Disassembly with One Wait State Cycle-Three Byte Transfer

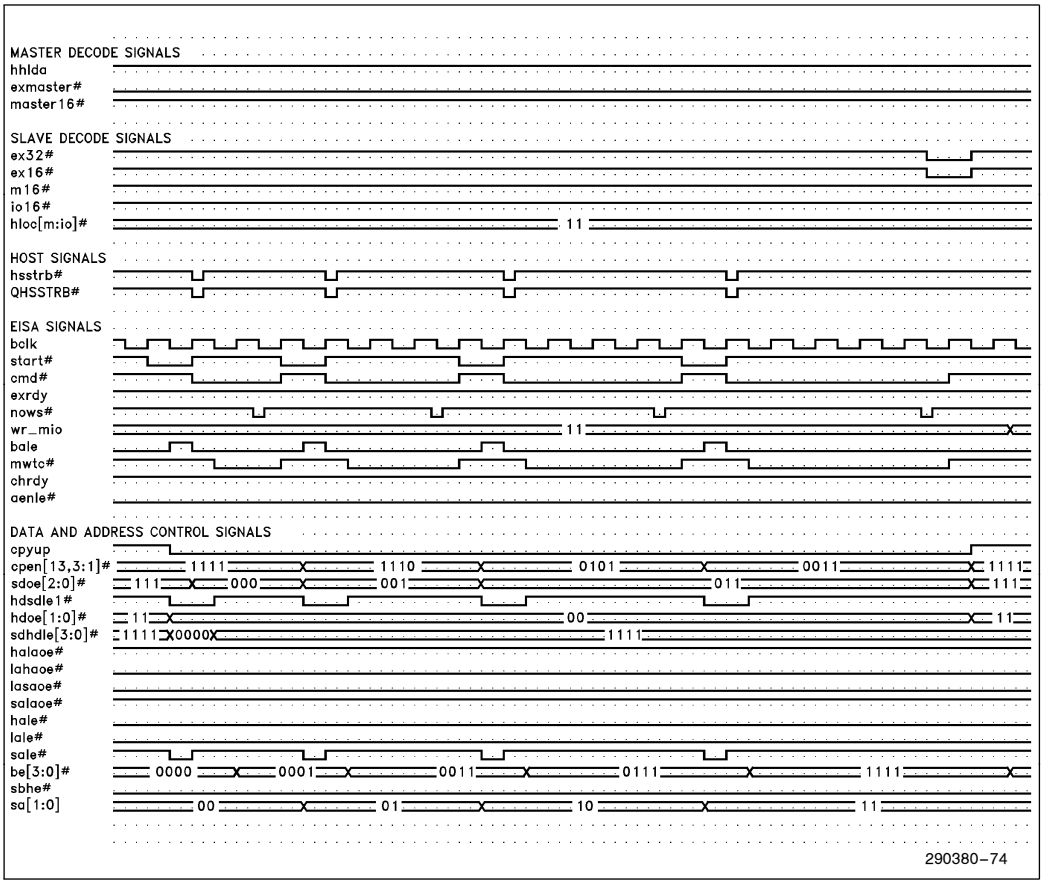


Figure 5-29. 32-Bit EISA Master to 8-Bit ISA Memory Slave NOWS# Disassembly Write Cycle-Four Byte Transfer

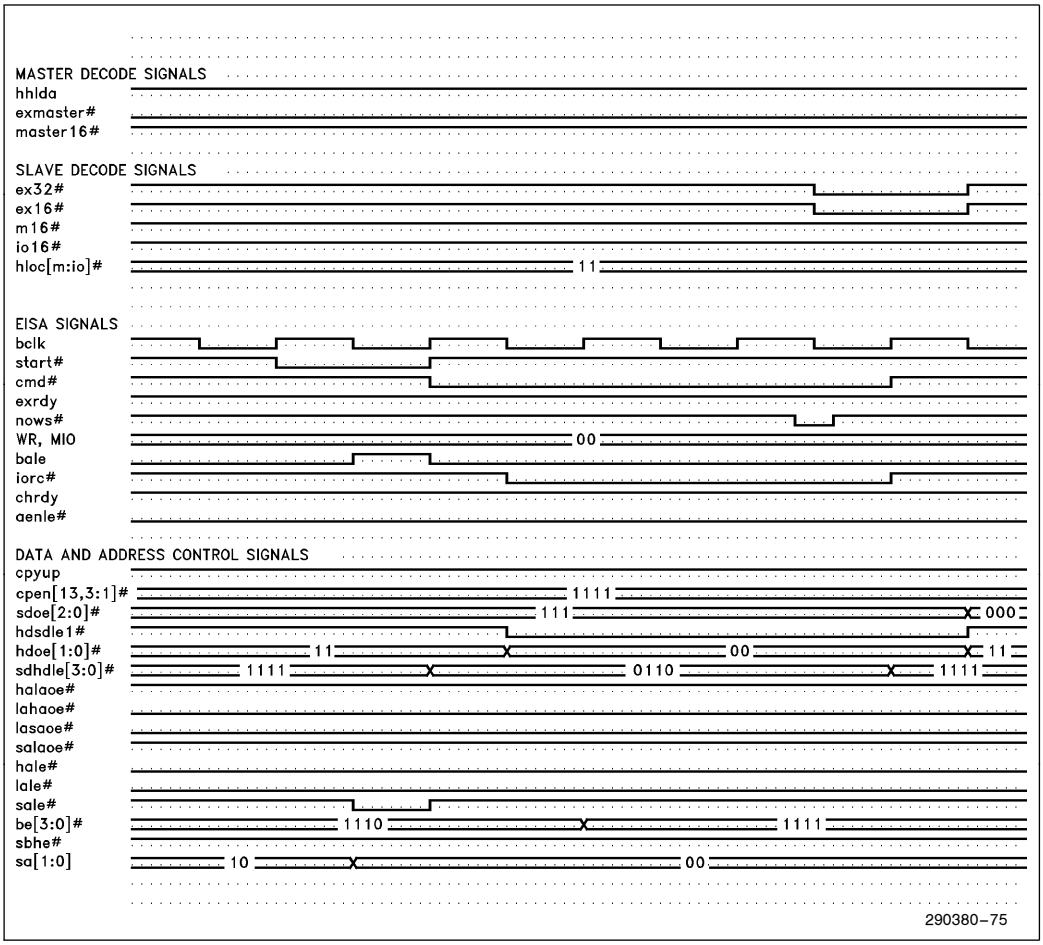


Figure 5-30. 32-Bit EISA Master to 8-Bit ISA I/O Slave NOWS# Standard Read Cycle-One Byte Transfer

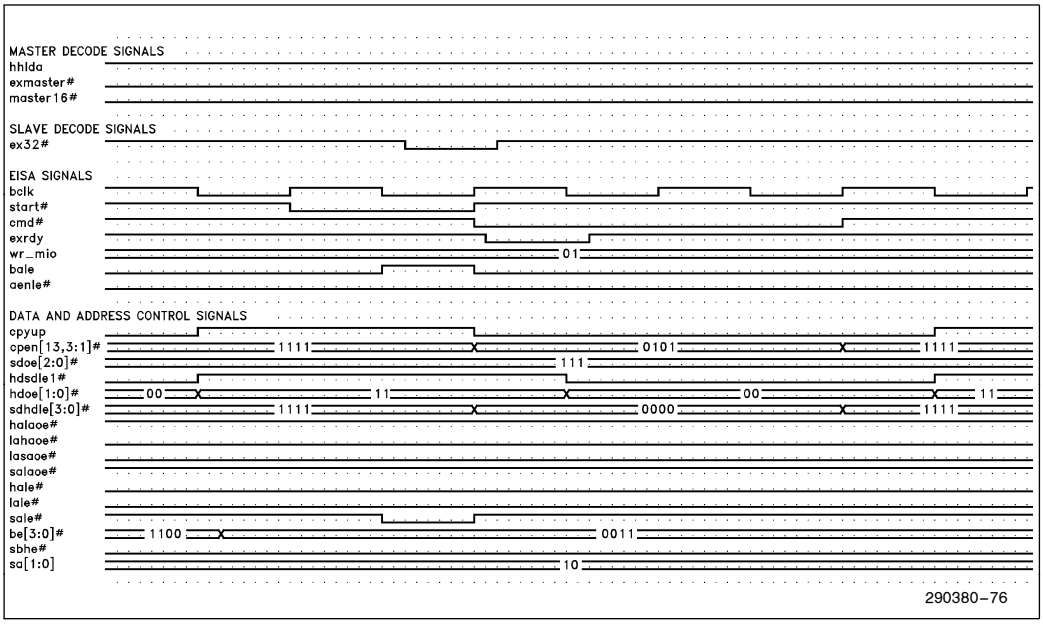


Figure 5-31. 16-Bit EISA Master to 32-Bit EISA Slave Read Cycle with One Wait State-Two Byte Transfer

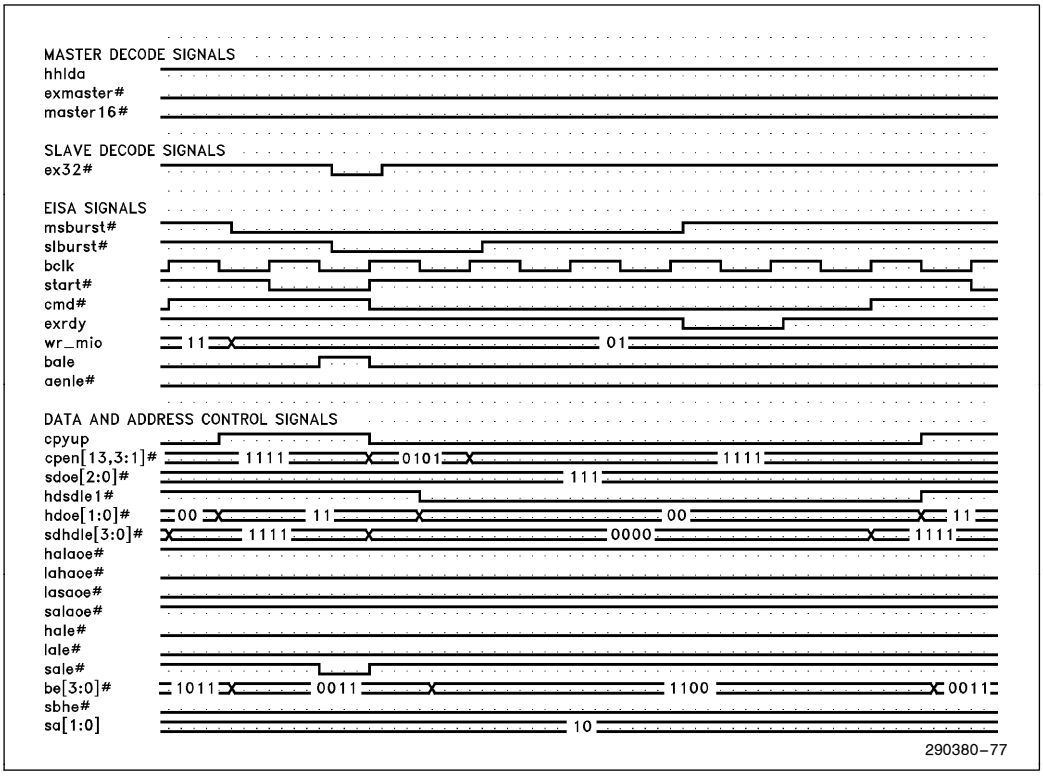


Figure 5-32. 16-Bit EISA Master to 32-Bit EISA Memory Burst Slave Read Cycle with One Wait State

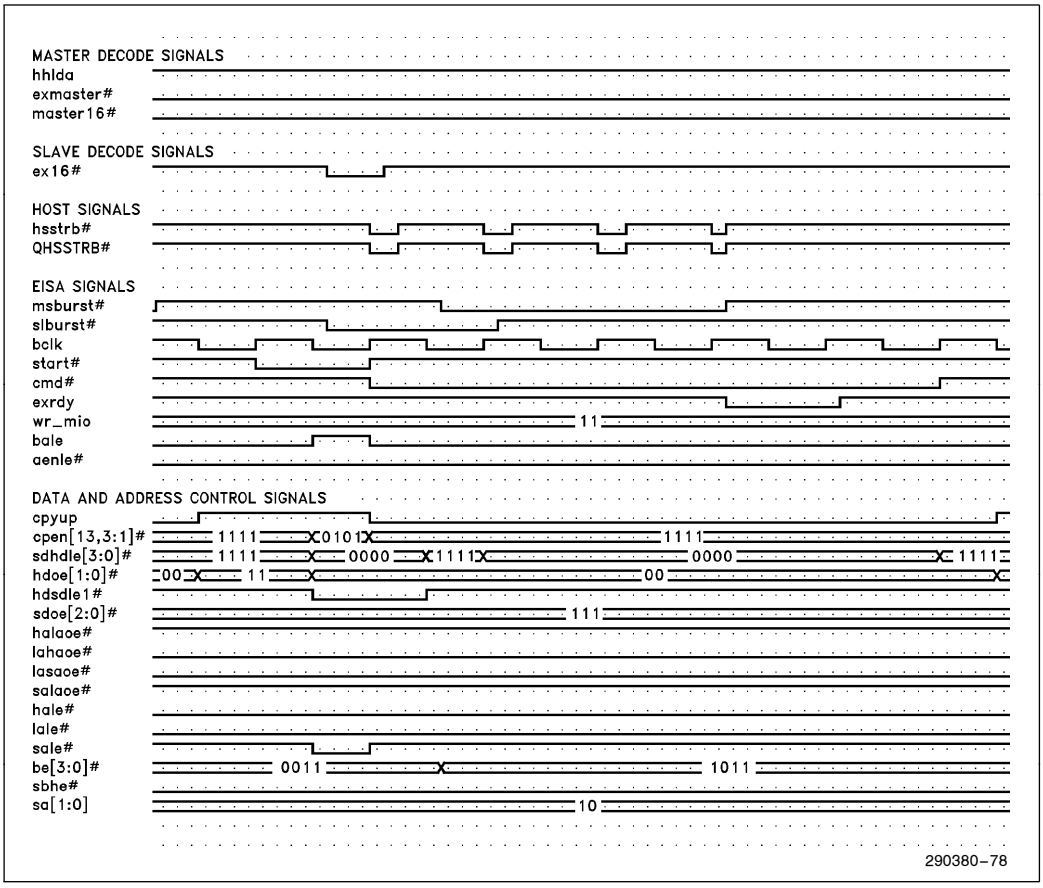


Figure 5-33. 16-Bit EISA Master to 16-Bit EISA Memory Slave Burst Write Cycle with One Wait State

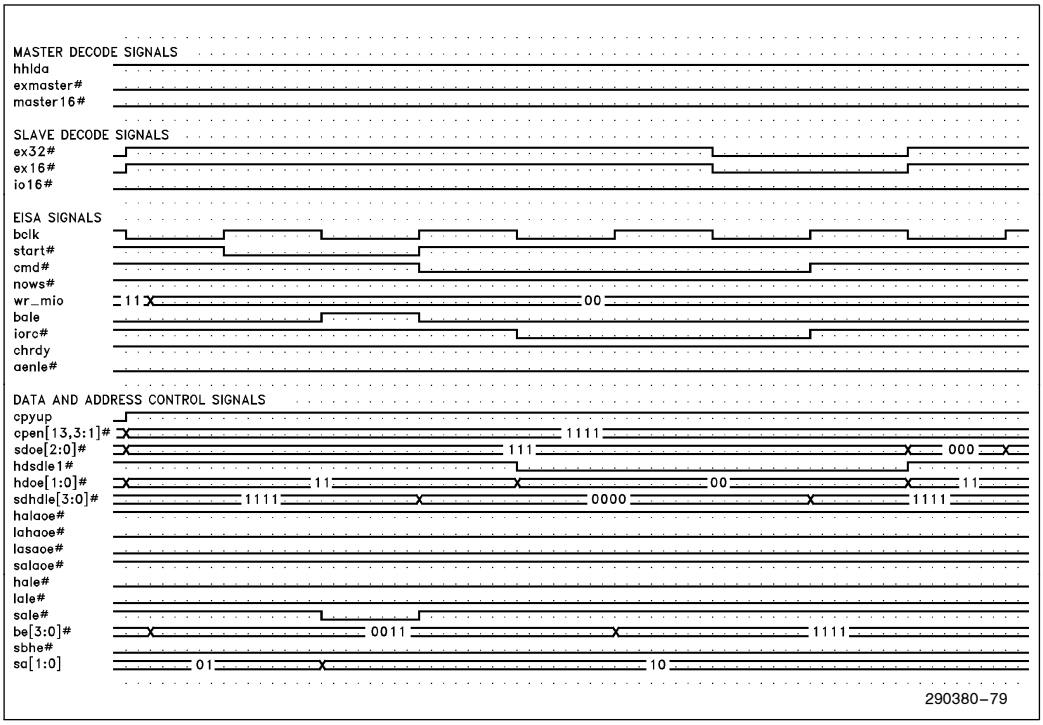


Figure 5-34. 16-Bit EISA Master to 16-Bit ISA I/O Slave Standard Read Cycle-Two Byte Transfer

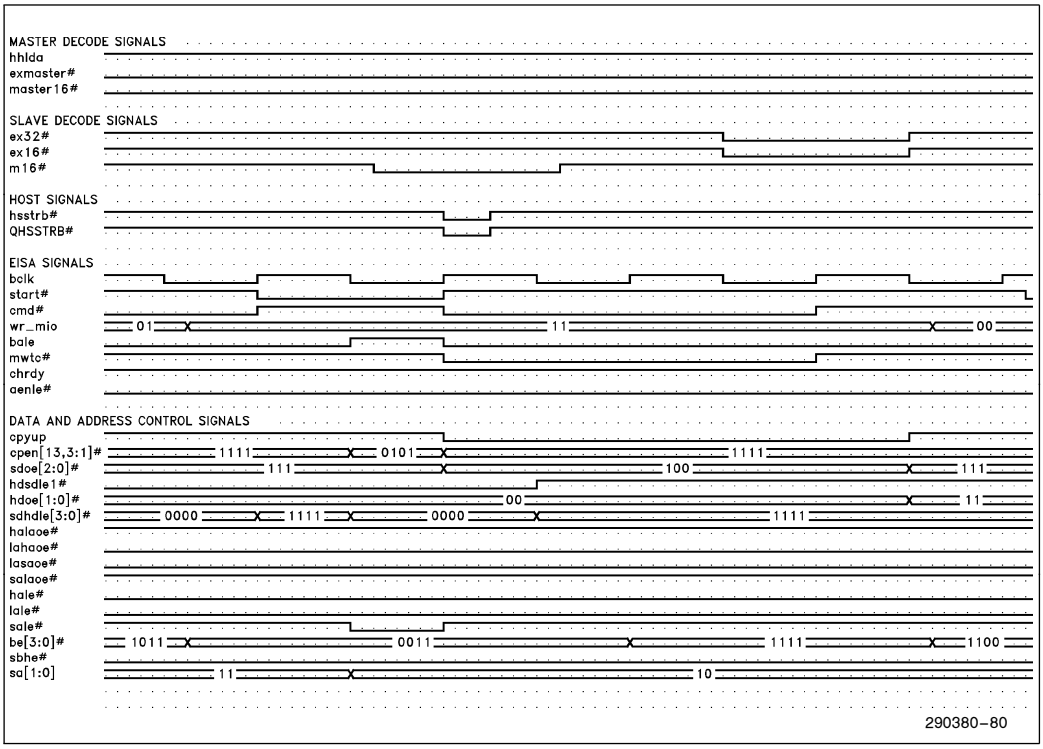


Figure 5-35. 16-Bit EISA Master to 16-Bit ISA Memory Slave Standard Write Cycle-Two Byte Transfer

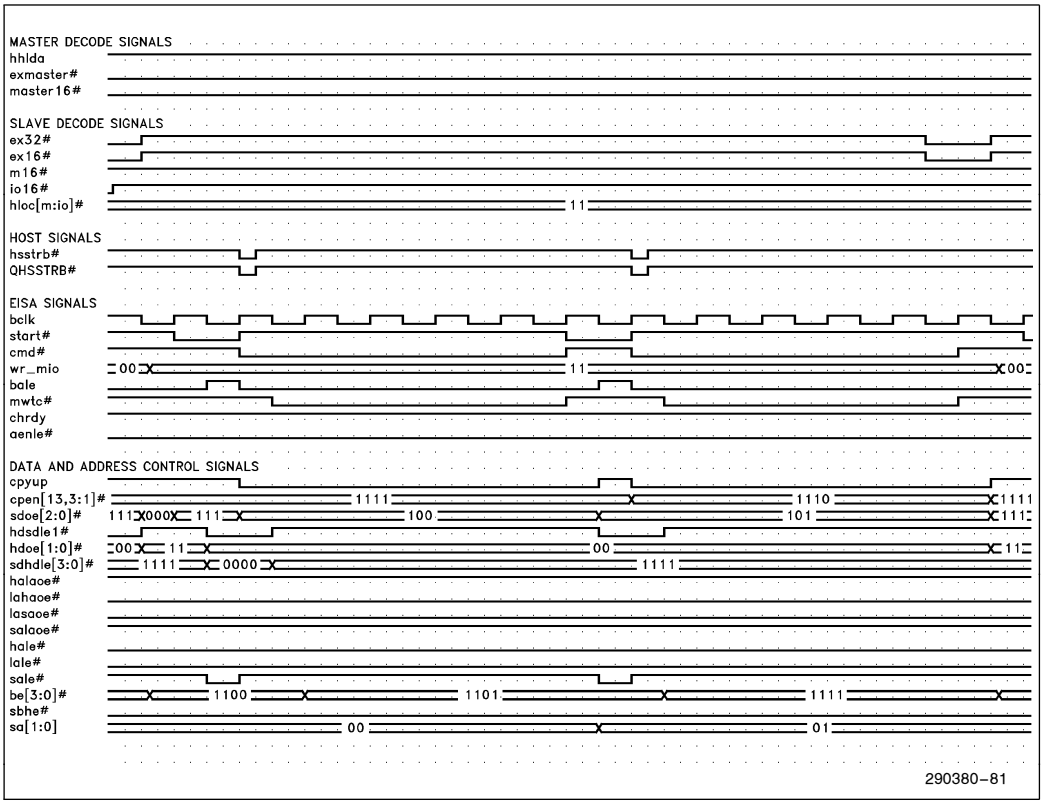


Figure 5-36. 16-Bit EISA Master to 8-Bit ISA Memory Slave Disassembly Write Cycle-Two Byte Transfer

5.5 ISA Master Cycles

[1]ISA masters gain access to the bus through a cascaded DMA channel. The ISA master asserts its ISA master request line (DREQx) to the system arbiter (82357/ISP). In sampling the ISA masters DREQx line active, the ISP, if the bus is currently available and the ISA master currently has highest priority, drives the ISA masters corresponding ISA master acknowledge (DACKx) signal active. Upon sampling the DACKx line active, the ISA master starts the cycle.

The beginning of cycle starts with the ISA bus master driving MASTER16# active to indicate to the 82358DT its 16-bit master status. [2]A BCLK later the ISA master places a valid address on the SA[19:0], LA[23:17], and SBHE# lines.

[3]After decoding the address as its own, the memory or I/O slave asserts the appropriate signals to indicate its slave type.

The ISA master then asserts one of the cycle control signals MRDC#, MWTC#, IORC#, or IOWC#, depending on the transfer (memory or I/O). [4]The 82358DT will automatically translate the ISA cycle to an EISA cycle (START#, CMD#, M-IO, and W-R), except in the case of an ISA master to an ISA memory slave or an ISA master to a host slave that does not assert EX32#. If the slave device is decoded as a 32-bit host or EISA slave, the 82358DT will perform data copying, if necessary (refer to Table 4-10).

The corresponding ISA cycle control signal (MRDC#, MWTC#, IORC#, or IOWC#) and EISA CMD# (if an EISA cycle is broadcasted) will remain active until the end of the cycle.

Wait states can be added by the slave device either by negating EXRDY (EISA/host slaves) or CHRDY (ISA slaves). The 82358DT samples EXRDY during ISA master cycles and translates it to CHRDY. *Note: It is not recommended to use HSTRETCH# to add wait states to an ISA master cycle, as HSTRETCH# stretches BCLK and an ISA master could be asynchronous to BCLK*.

If the ISA master must run Refresh cycles before it relinquishes the bus, it floats the address lines and cycle control signals and asserts REFRESH# to the ISP and 82358DT. The ISP generates the address and the 82358DT generates the cycle control signals. The 82358DT broadcasts both EISA and ISA cycles during a refresh. The ISA master must then wait one BCLK period after MRDC# is negated before floating refresh and driving the address lines and cycle control signals.

NOTES:

(1) An ISP's DMA channel must be programmed for cascade mode in order for a 16-bit ISA master to gain access to the EISA/ISA bus. ISA masters use the DREQx and DACKx lines as their master request and master acknowledge signals (refer to the ISP data sheet).

(2) Some ISA masters may drive a valid address on the SA[19:0], LA[23:17], and SBHE# lines simultaneously with MASTER16#.

The 82358DT controls the propagation of the SA[19:2] address through the address buffers onto the LA and HA buses. The 82358DT translates the SBHE#, SA0, and SA1 lines to HBE[3:0]# and BE[3:0]#.

(3) An EISA slave will assert either EX16# (indicating 16-bit EISA memory or I/O), or EX32# (indicating 32-bit EISA memory or I/O), depending on its data bus size. If the slave device is 8-bits, neither EX16# nor EX32# will be asserted.

An ISA slave will assert either M16# (indicating 16-bit ISA memory), or IO16# (indicating 16-bit I/O). If the slave device is 8-bits, neither M16# nor IO16# will be asserted. The ISA slave will also assert NOWS#, (after one of the ISA control signals has been asserted), if no wait state cycles are supported.

A host slave will assert either HLOCMEM# (indicating 32-bit host memory), or HLOCIO# (indicating 32-bit host I/O). If the host slave is an I/O device, the 82358DT will assert IO16#, indicating to the ISA master that the host slave can support 16-bit ISA I/O cycles. If the host slave is a memory device, and the host slave supports ISA cycles, the system board must assert M16#, indicating to the ISA master that the host slave can support 16-bit ISA memory cycles.

Refer to section 4.3 for additional information regarding slave/master decode.

(4) If the 82358DT, when sampling the slave decode signals, determines that the slave device is an 8 or 16-bit ISA memory, no EISA cycle will be broadcasted (refer to Table 4-9).

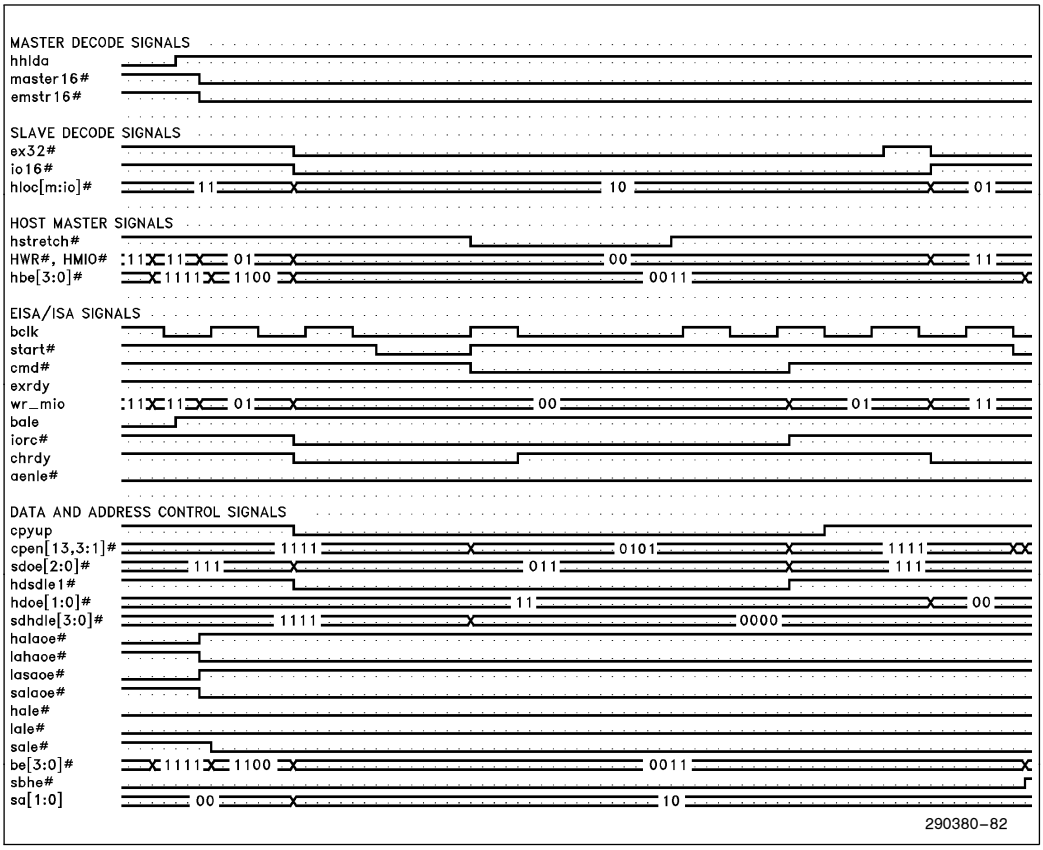


Figure 5-37. 16-Bit ISA Master to Host I/O Slave Read Cycle with HSTRETCH# and One Wait State-Two Byte Transfer

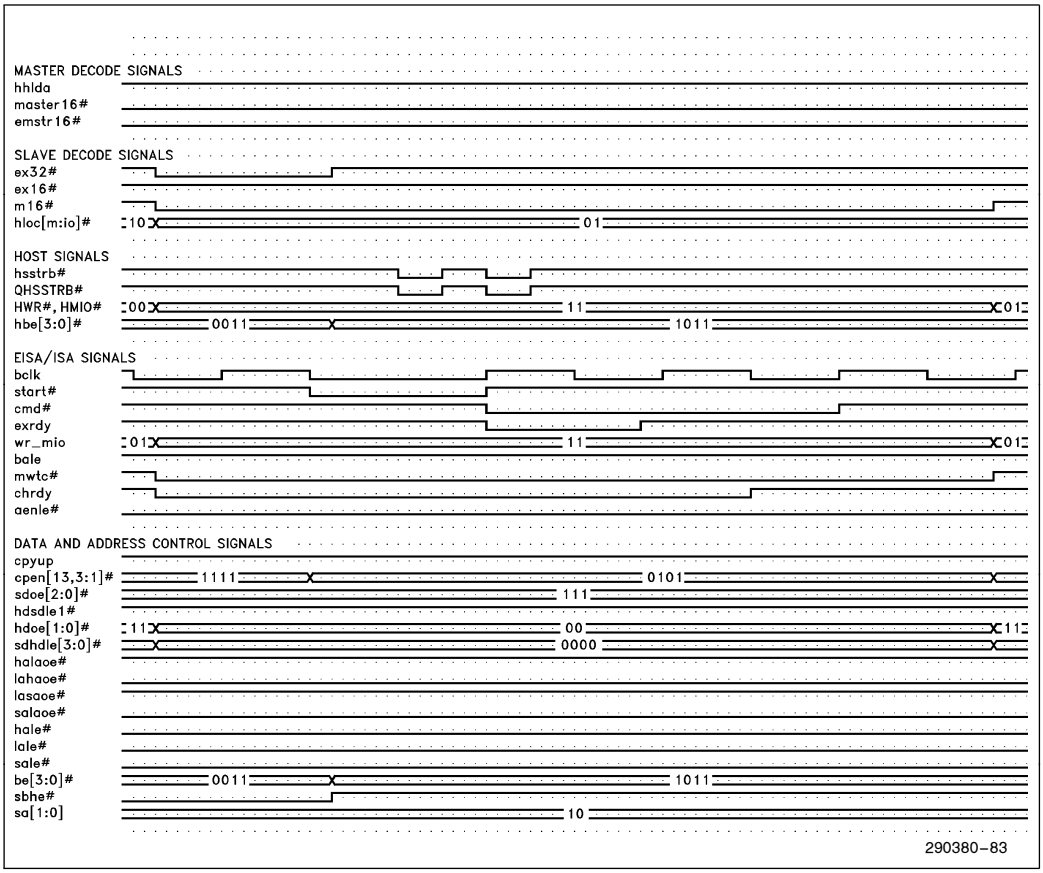


Figure 5-38. 16-Bit ISA Master to Host Memory Slave Standard Write Cycle with One Wait State-One Byte Transfer

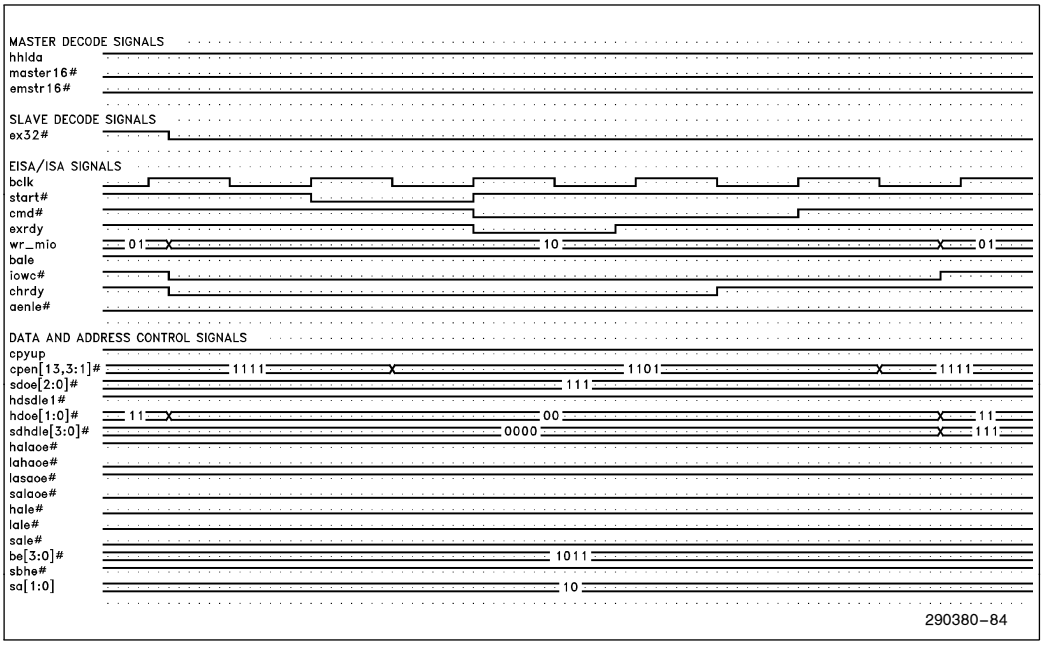


Figure 5-39. 16-Bit ISA Master to 32-Bit EISA I/O Slave Write Cycle with One Wait State-One Byte Transfer

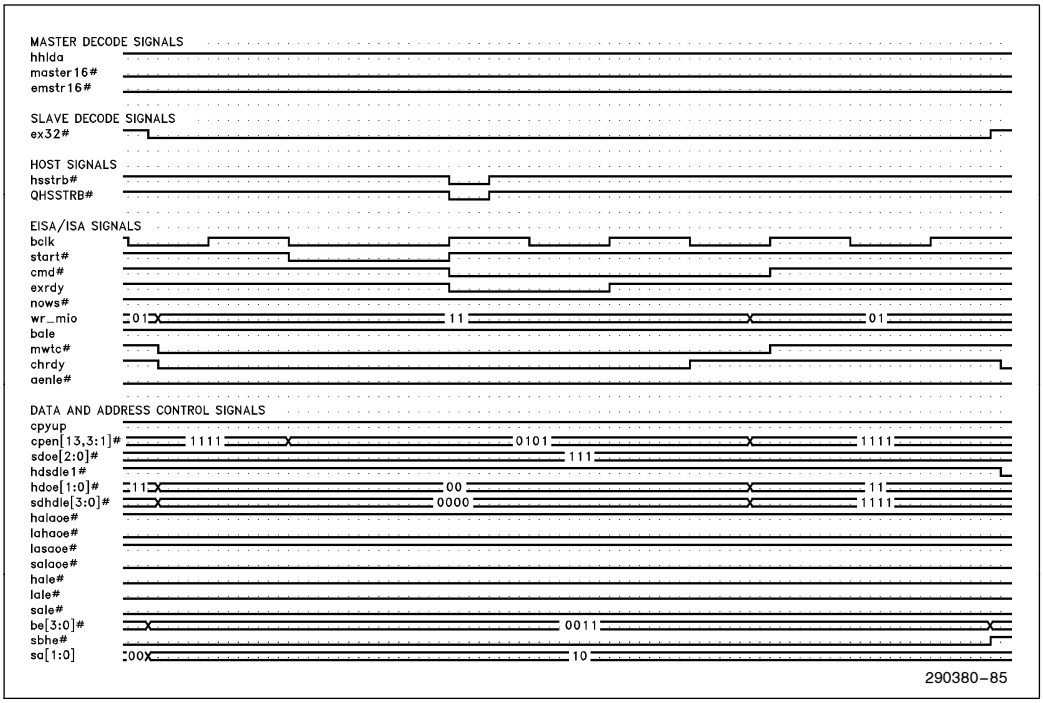


Figure 5-40. 16-Bit ISA Master to 32-Bit EISA Memory Slave Write Cycle with One Wait State-Two Byte Transfer

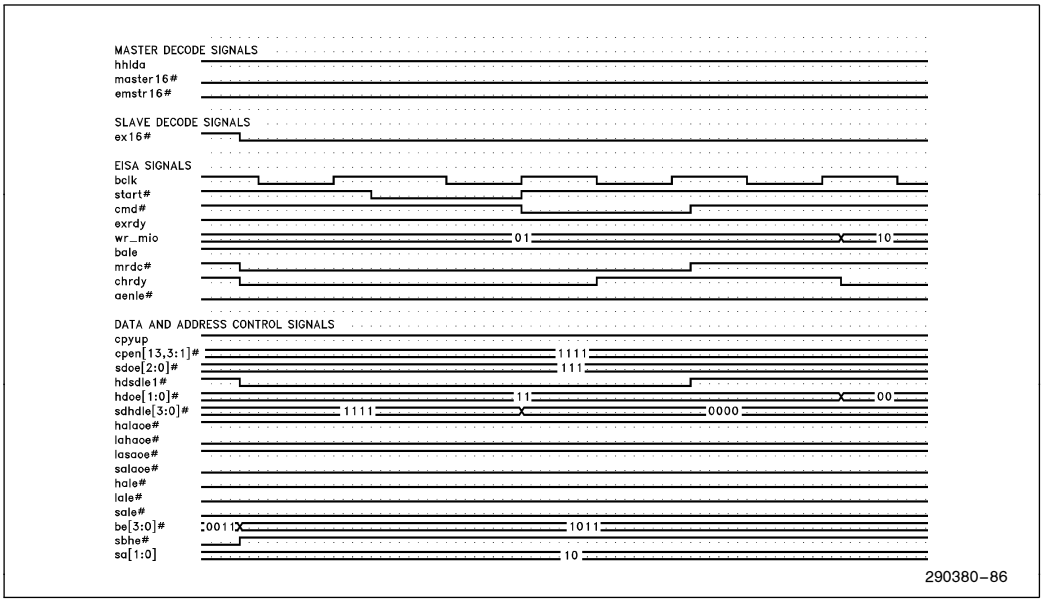


Figure 5-41. 16-Bit ISA Master to 16-Bit EISA Memory Slave Standard Read Cycle-One Byte Transfer

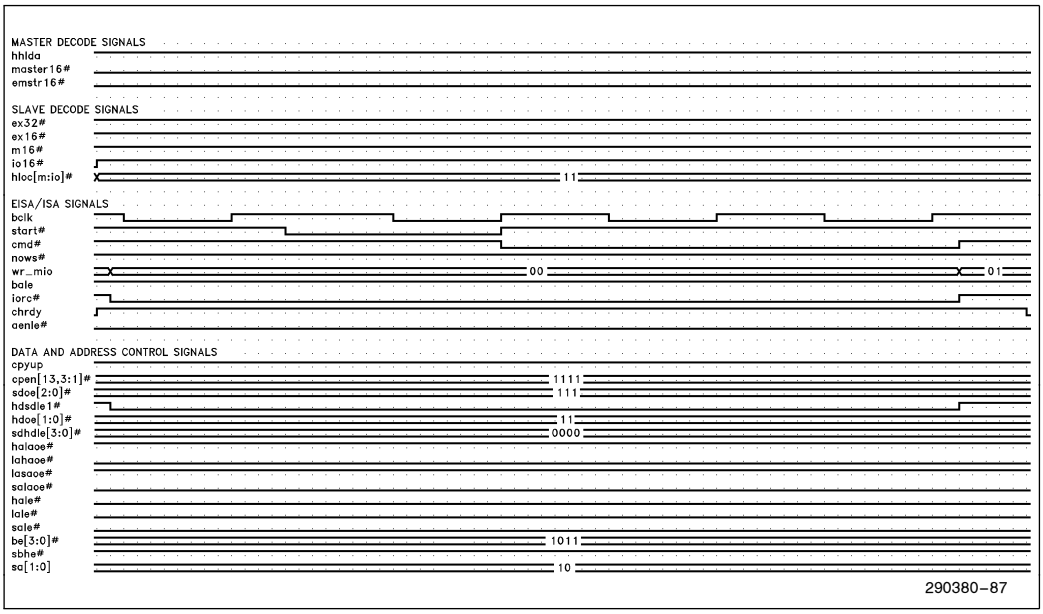


Figure 5-42. 16-Bit ISA Master to 8-Bit ISA I/O Slave Standard Read Cycle-One Byte Transfer

5.6 DMA Cycles

There are four types of DMA cycles that can be generated: compatible, type ''A'', type ''B'', and burst type ''C'' cycles. The 82358DT supports 8-, 16-, and 32-bit DMA transfers. The ISP generates the address and the 82358DT controls the transfer. DMA cycles are generated as fly-by transfers (i.e., the memory and I/O are accessed simultaneously).

DMA devices monitor EXRDY, and IORC# or IOWC# during read and write cycles. Memory slaves use either HW/R#, W-R, MRDC#, MWTC#, SMRDC#, SMWTC#, and/or CMD# and START#, depending on the slave type (Host, EISA, or ISA). MRDC# or MWTC# is generated whenever the memory that responds is ISA memory or the DMA cycle type is compatible (note: MRDC# and MWTC# are not generated during compatible DMA cycles if EISA memory responds and HGT16M# is asserted). SMWTC# or SMWTC# is generated whenever the memory that responds is ISA memory and the address is 1 Mbyte or less (i.e., GT1M# is sampled inactive). HW-R#, W-R, START#, and CMD# are always generated.

To initiate a DMA transfer, the ISP must be programmed with the DMA devices (i.e., I/O devices) data size and DMA cycle type. The cycle starts with the ISP placing a valid address, BE[3:0]#, HW/R#, and ST[3:0] value on the bus. The ST[3:0] lines are used to transfer the DMA devices size and cycle type to the 82358DT.

The 82358DT then drives START# active to indicate start of cycle. The slave decode signals are sampled during START# to determine the memory slaves size and type (Host, EISA, or ISA). CMD# and the ISA cycle control signals are then asserted. If the DMA cycle is a write to memory, the ISA cycle control signal IORC# will be asserted on the rising edge of BCLK after the address is placed on the bus.

CMD# and the corresponding ISA cycle control signal are held active until the end of the cycle. Wait states can be added by the memory slave device either by negating EXRDY (Host or EISA slaves) or CHRDY (ISA slaves). DMA devices can not add wait states. A host slave cycle may also be extended by driving HSTRETCH# low. The cycle will be extended until HSTRETCH# is driven inactive (refer to section 4.9).

If the memory size is less than the I/O size, assembly/disassembly, copying, and data re-drive are provided if necessary, except when compatible timing is selected. In the case of compatible timing, single cycles with copying, if necessary, is provided (i.e., no assembly or disassembly is done). Refer to Table 4-10 for additional information on data size translations during DMA cycles.

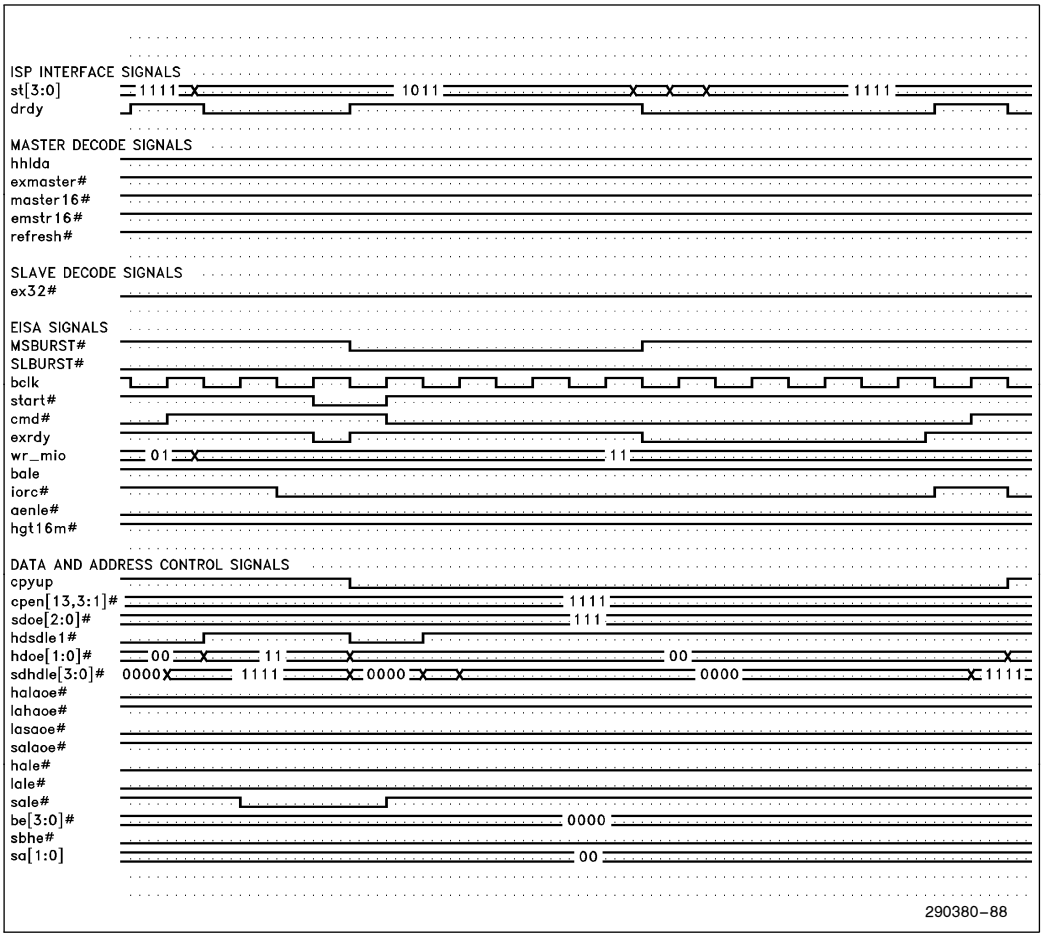


Figure 5-43. 32-Bit I/O to 32-Bit Memory Burst Write DMA Cycle

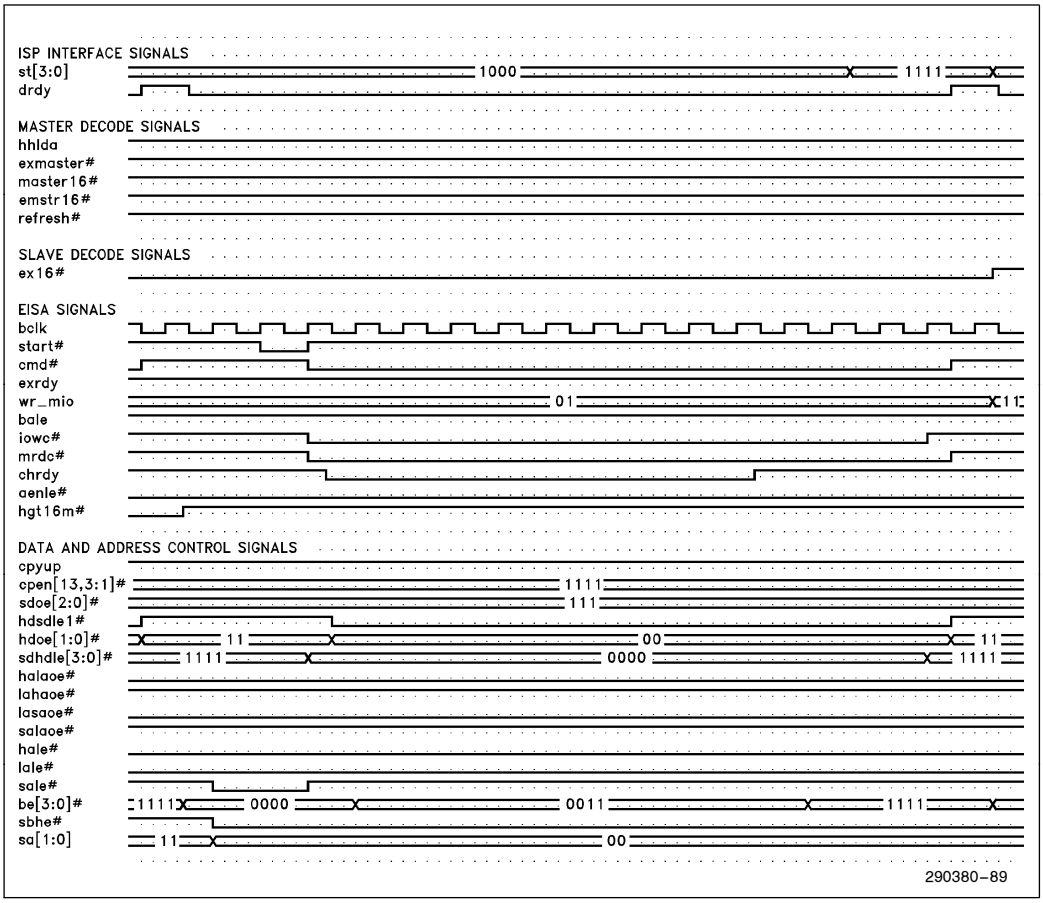


Figure 5-44. 32-Bit I/O to 16-Bit Memory Standard Read Compatible DMA Cycle with Nine Wait States-Two Byte Transfer

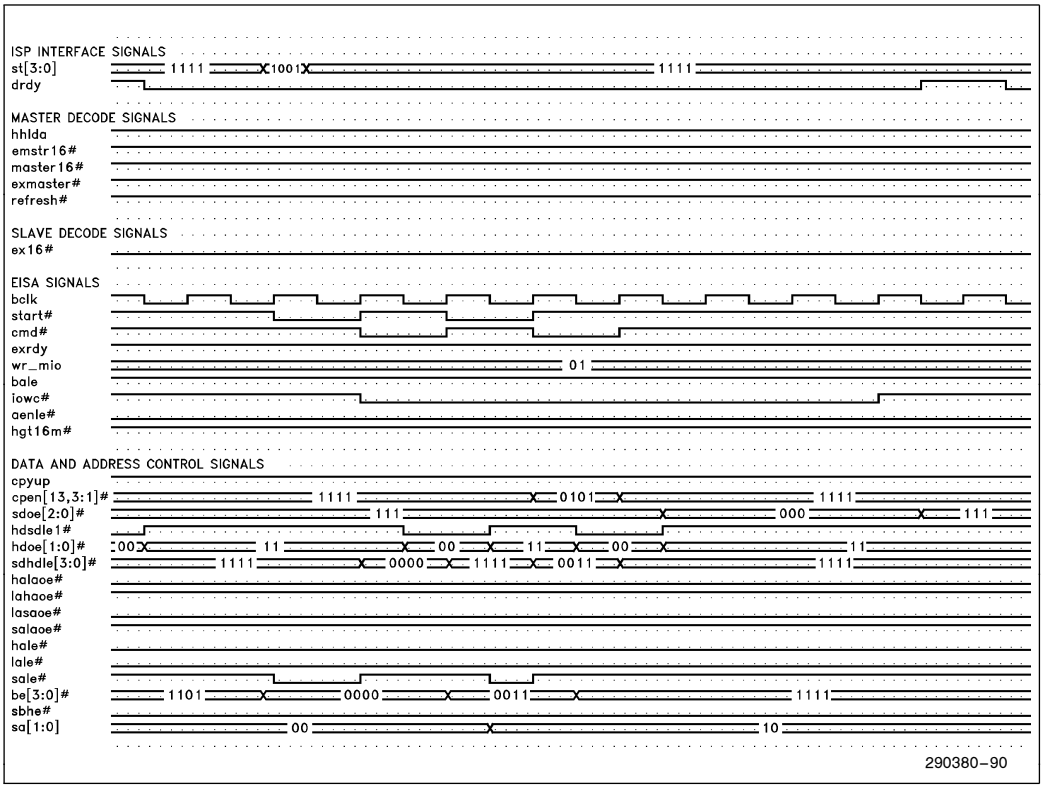


Figure 5-45. 32-Bit I/O to 16-Bit Memory Assembly Read Type A DMA Cycle-Four Byte Transfer

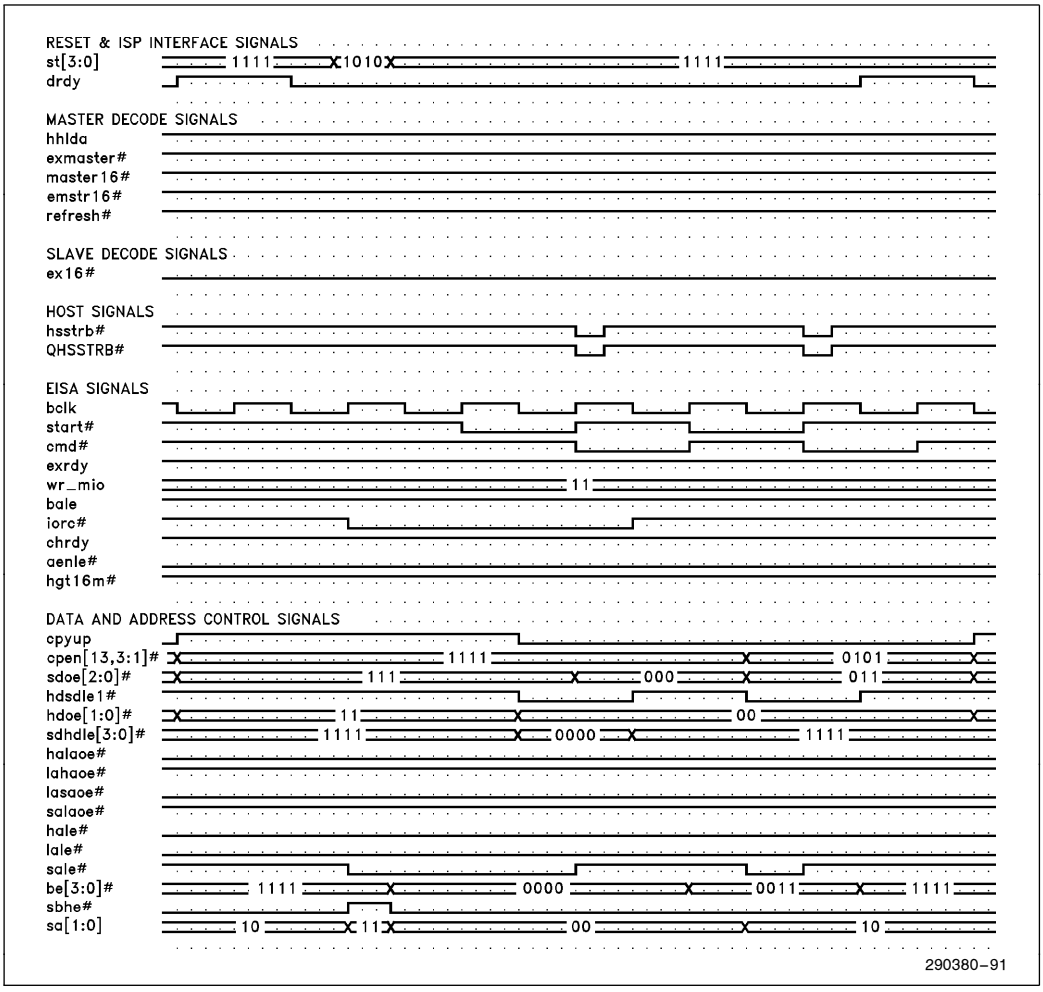


Figure 5-46. 32-Bit I/O to 16-Bit Memory Disassembly Write Type B DMA Cycle-Four Byte Transfer

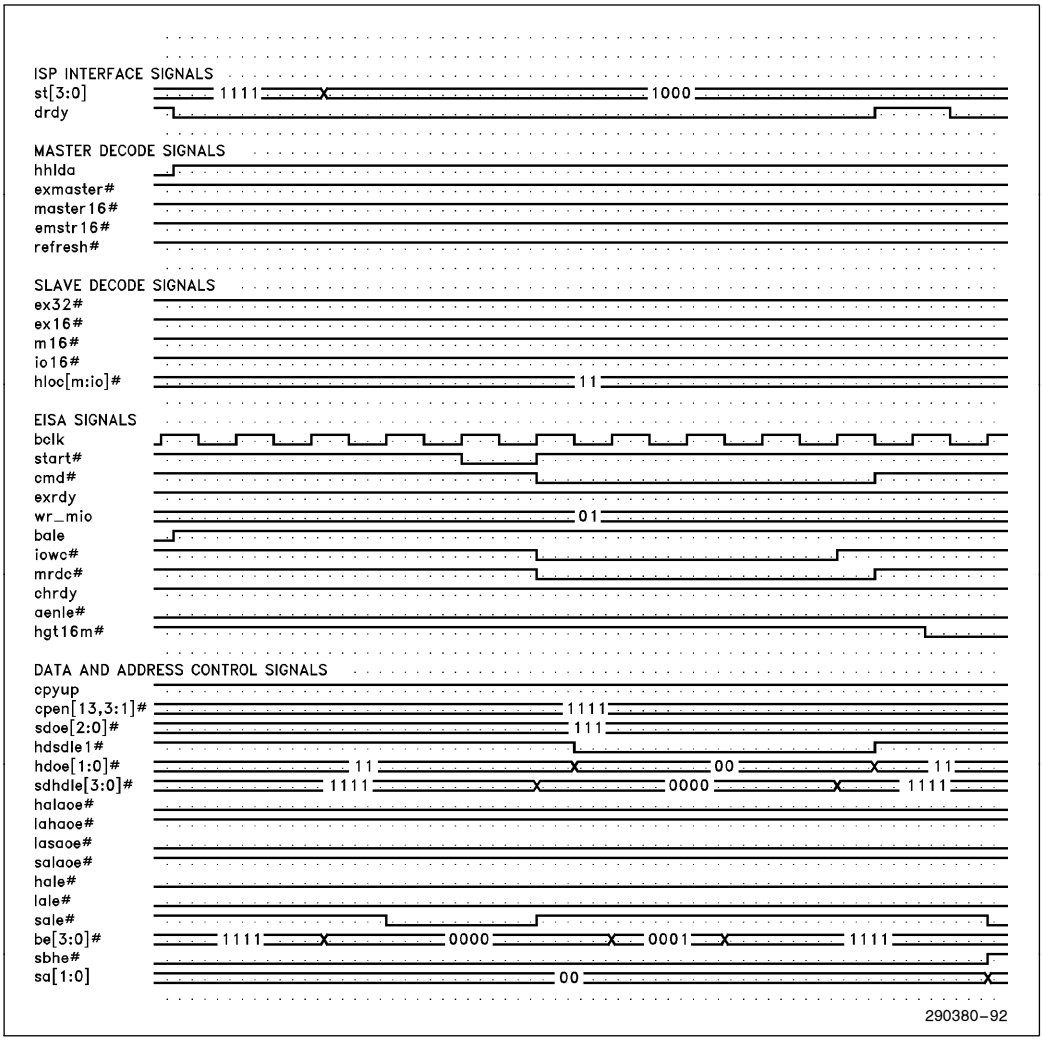


Figure 5-47. 32-Bit I/O to 8-Bit Memory Slave Standard Read Compatible DMA Cycle-One Byte Transfer

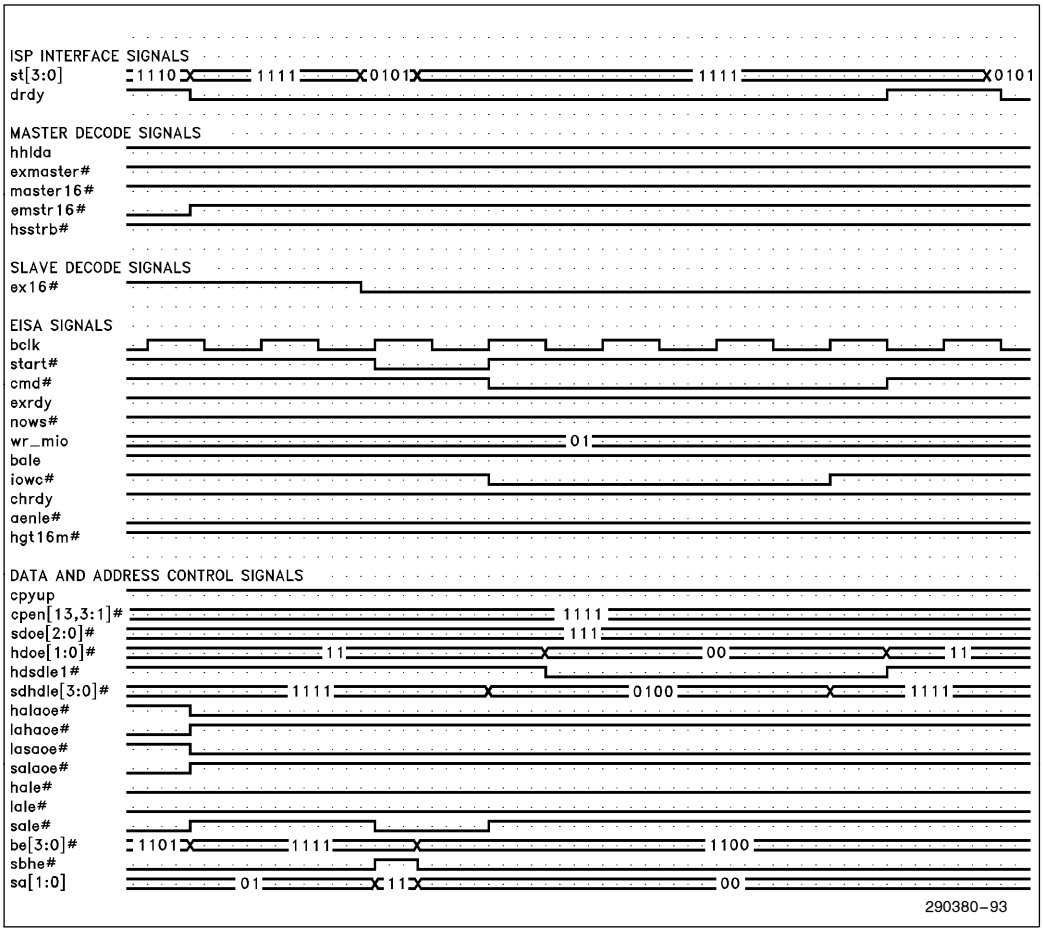


Figure 5-48. 16-Bit I/O to 16-Bit Memory Standard Read Type A DMA Cycle-Two Byte Transfer

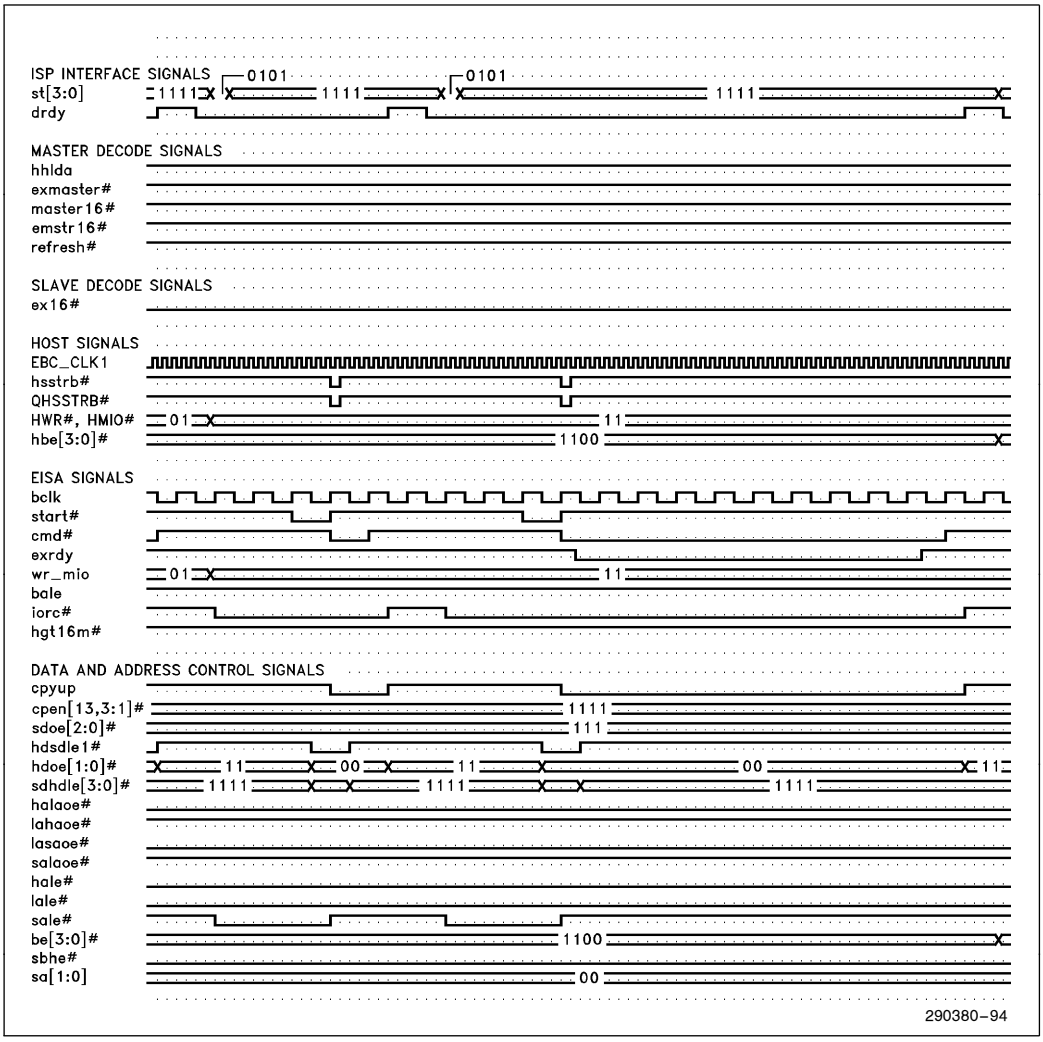


Figure 5-49. 16-Bit I/O to 16-Bit Memory Slave Type A Cycles with and without Wait States-Two Byte Transfers

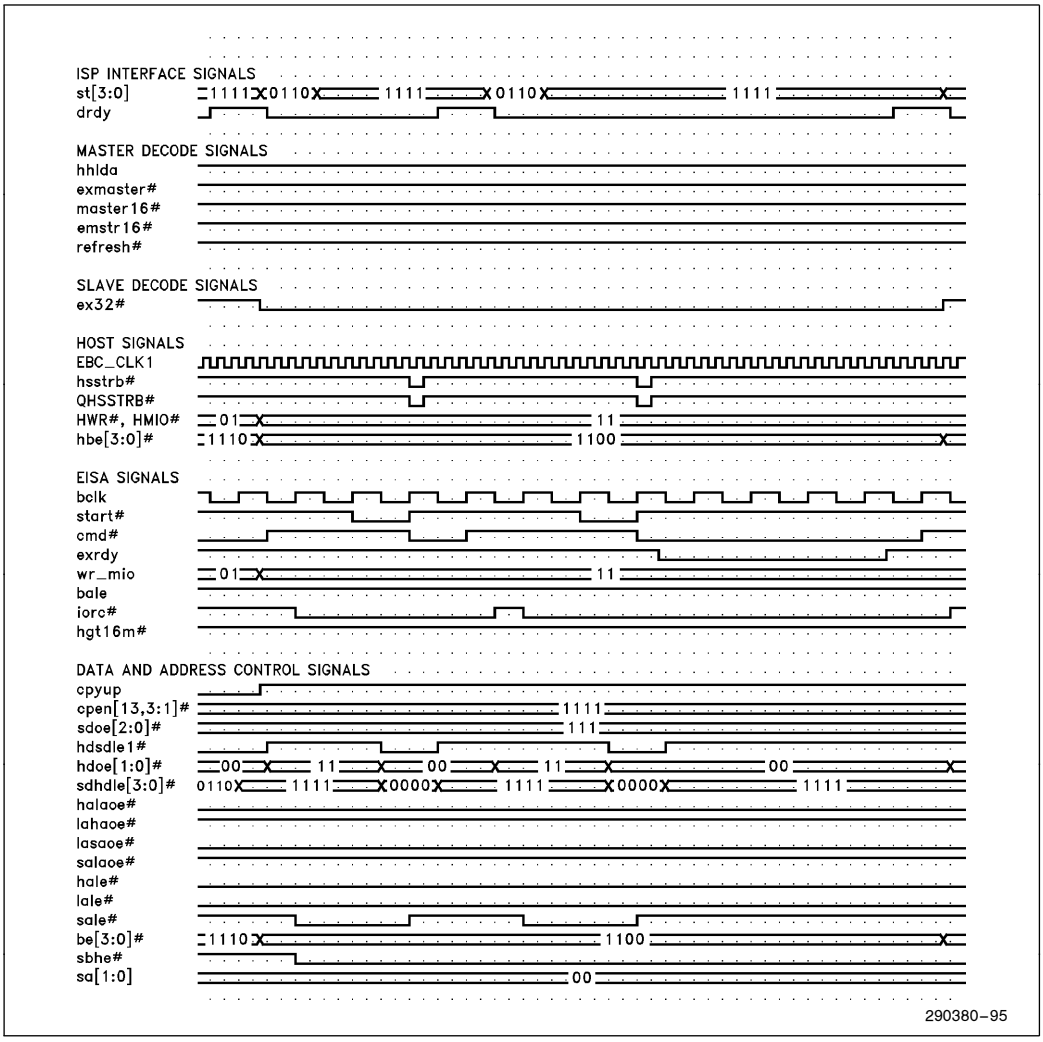


Figure 5-50. 16-Bit I/O to 32-Bit Memory Slave Type B Cycles with and without Wait States-Two Byte Transfers

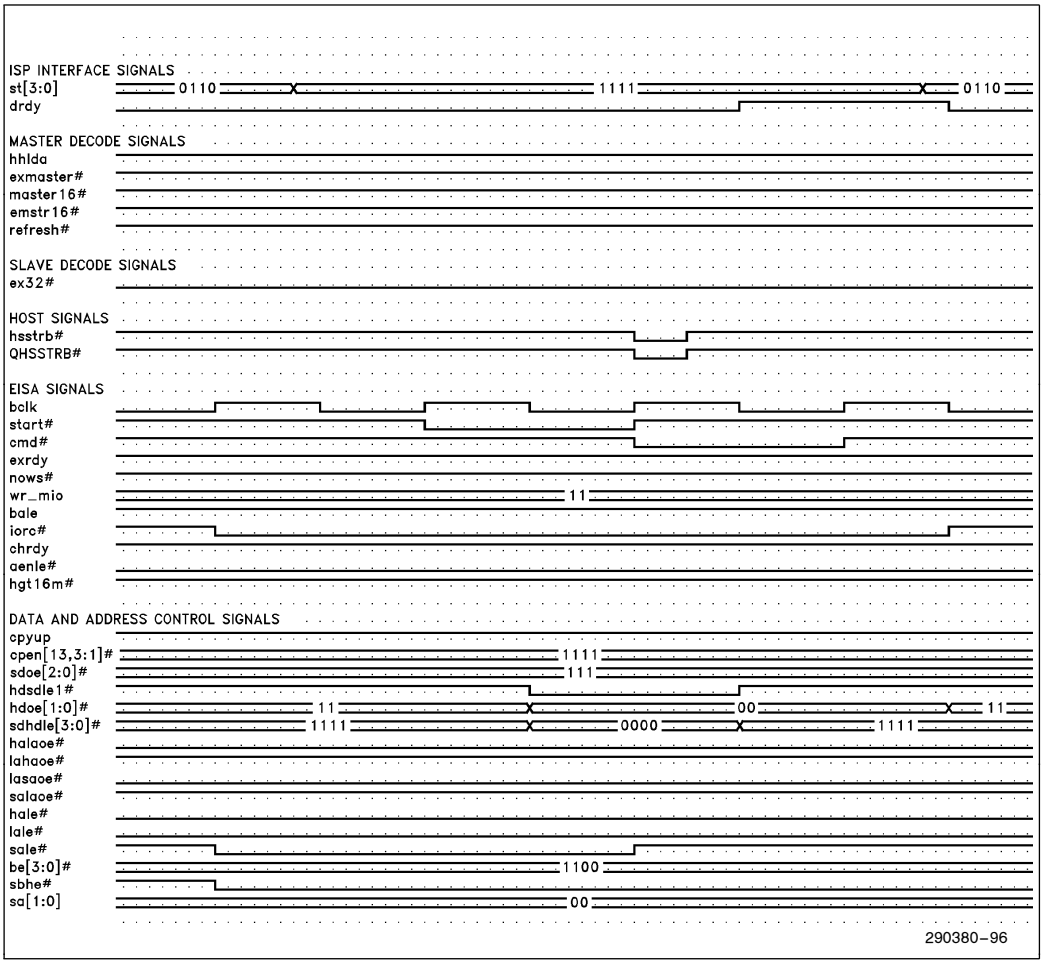


Figure 5-51. 16-Bit I/O to 32-Bit Memory Standard Write Type B DMA Cycle-Two Byte Transfer

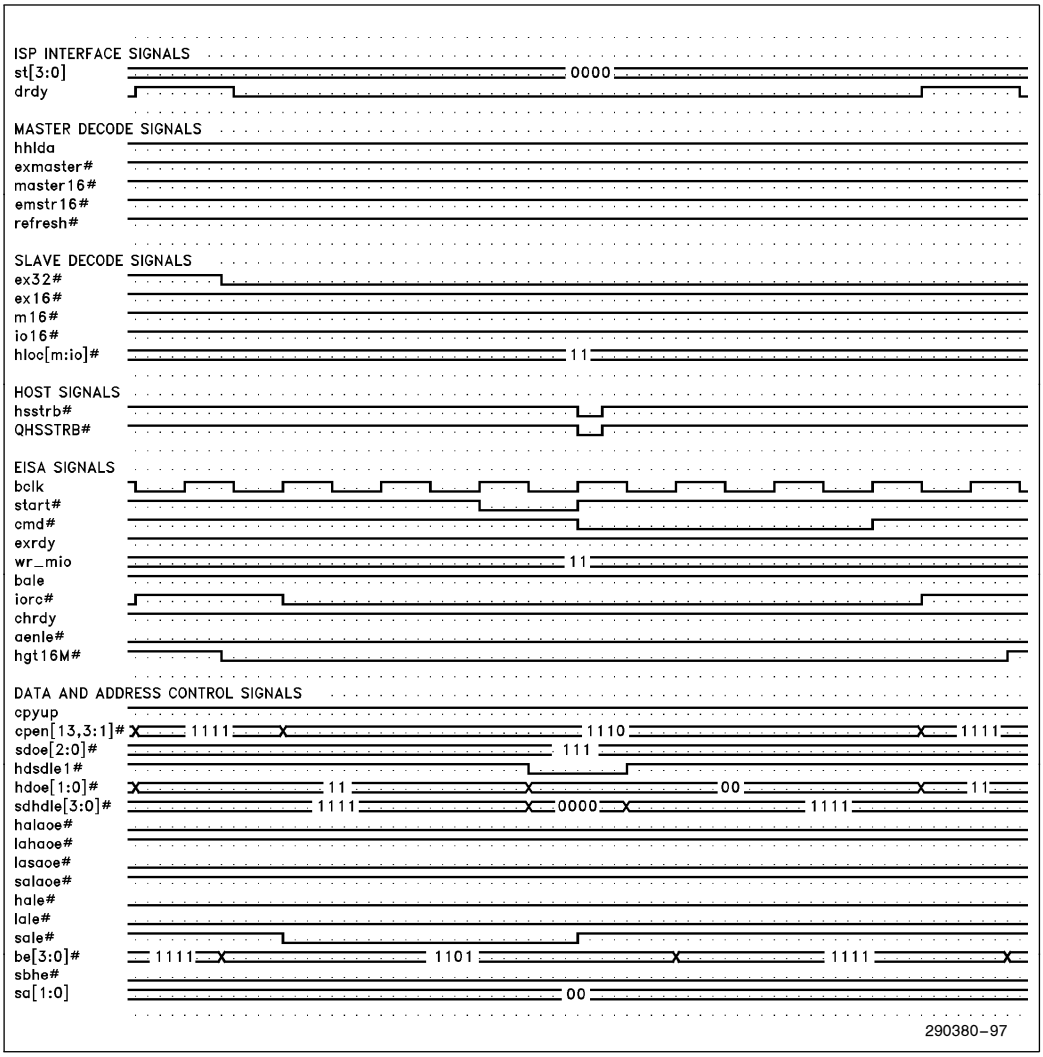


Figure 5-52. 8-Bit I/O to 32-Bit Memory Compatible Standard Write DMA Cycle-One Byte Transfer

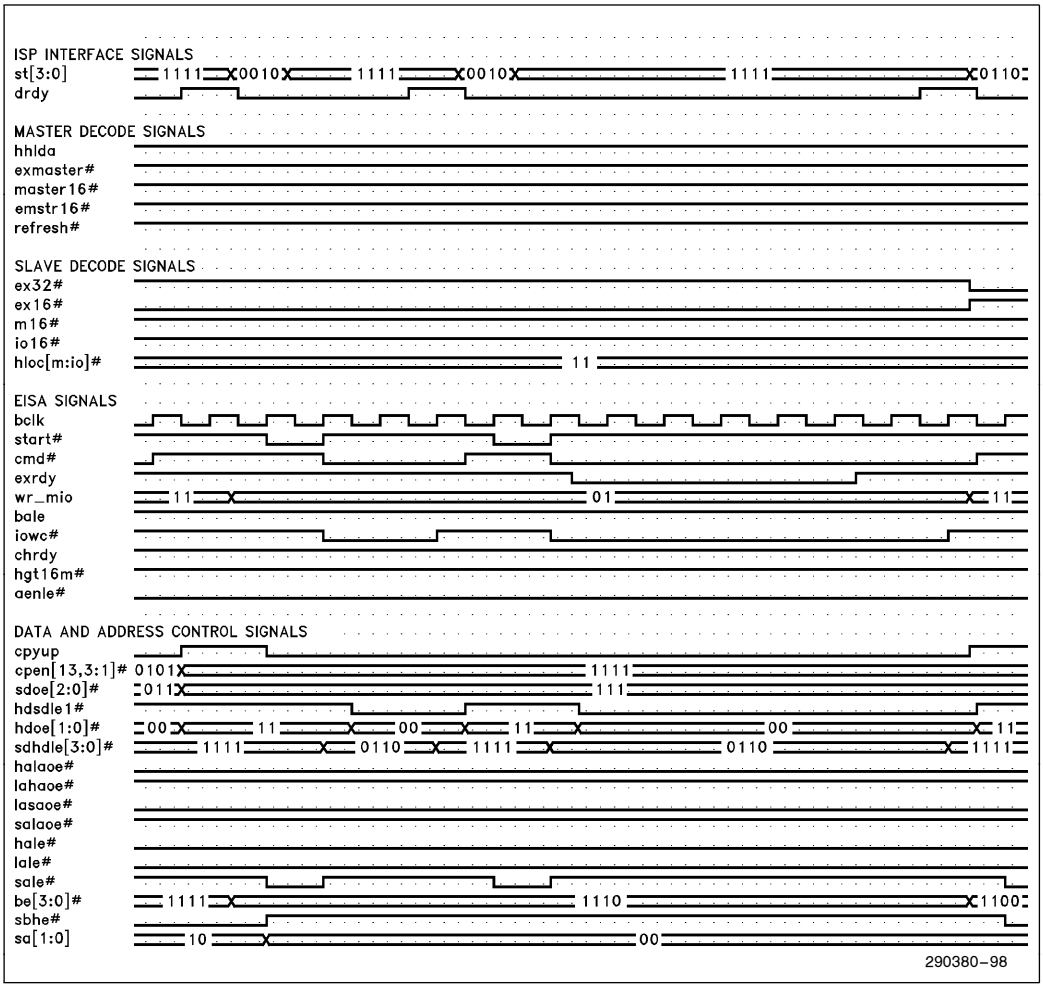


Figure 5-53. 8-Bit I/O to 16-Bit Memory Back-to-Back Standard Read Type B DMA Cycles with Five Wait States-One Byte Transfers

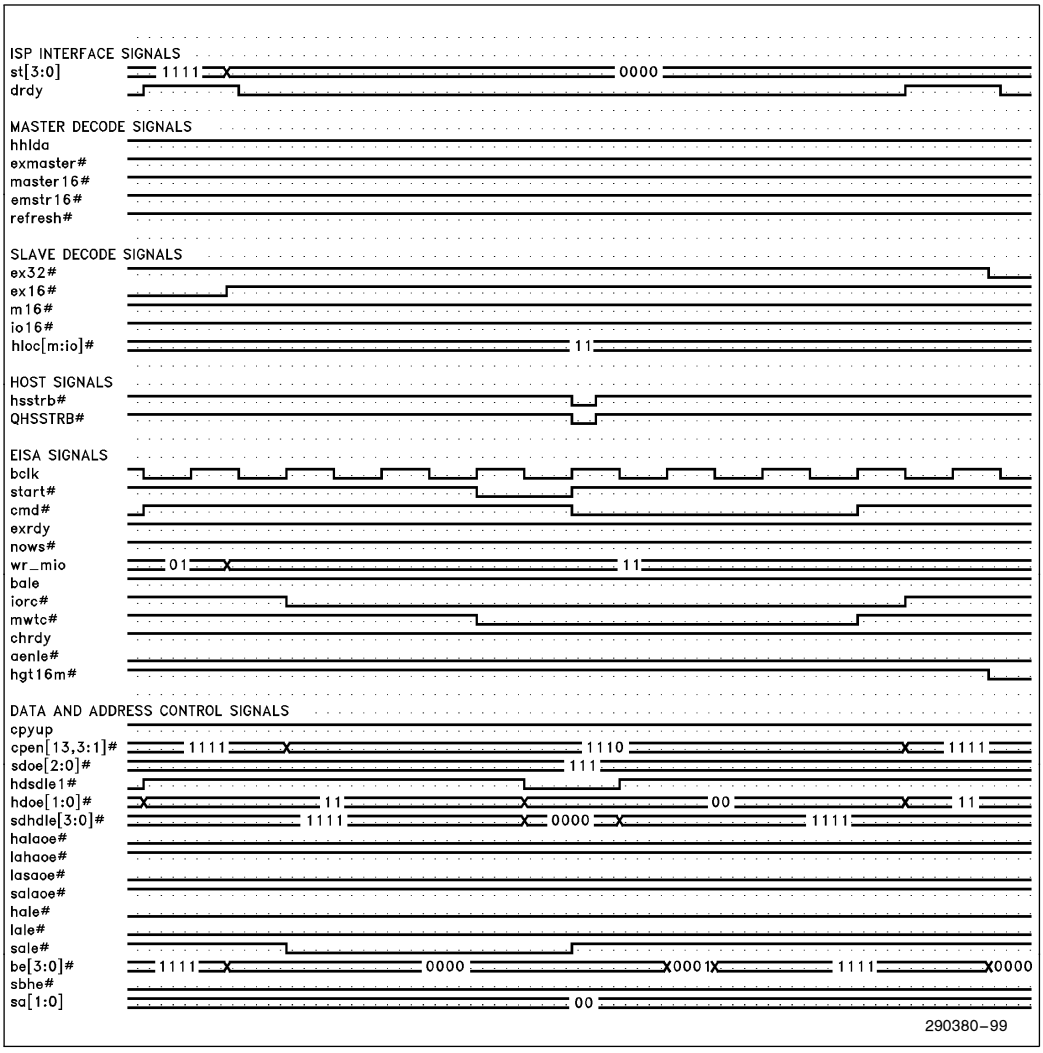


Figure 5-54. 8-Bit I/O to 8-Bit Memory Standard Write Compatible DMA Cycle-One Byte Transfer

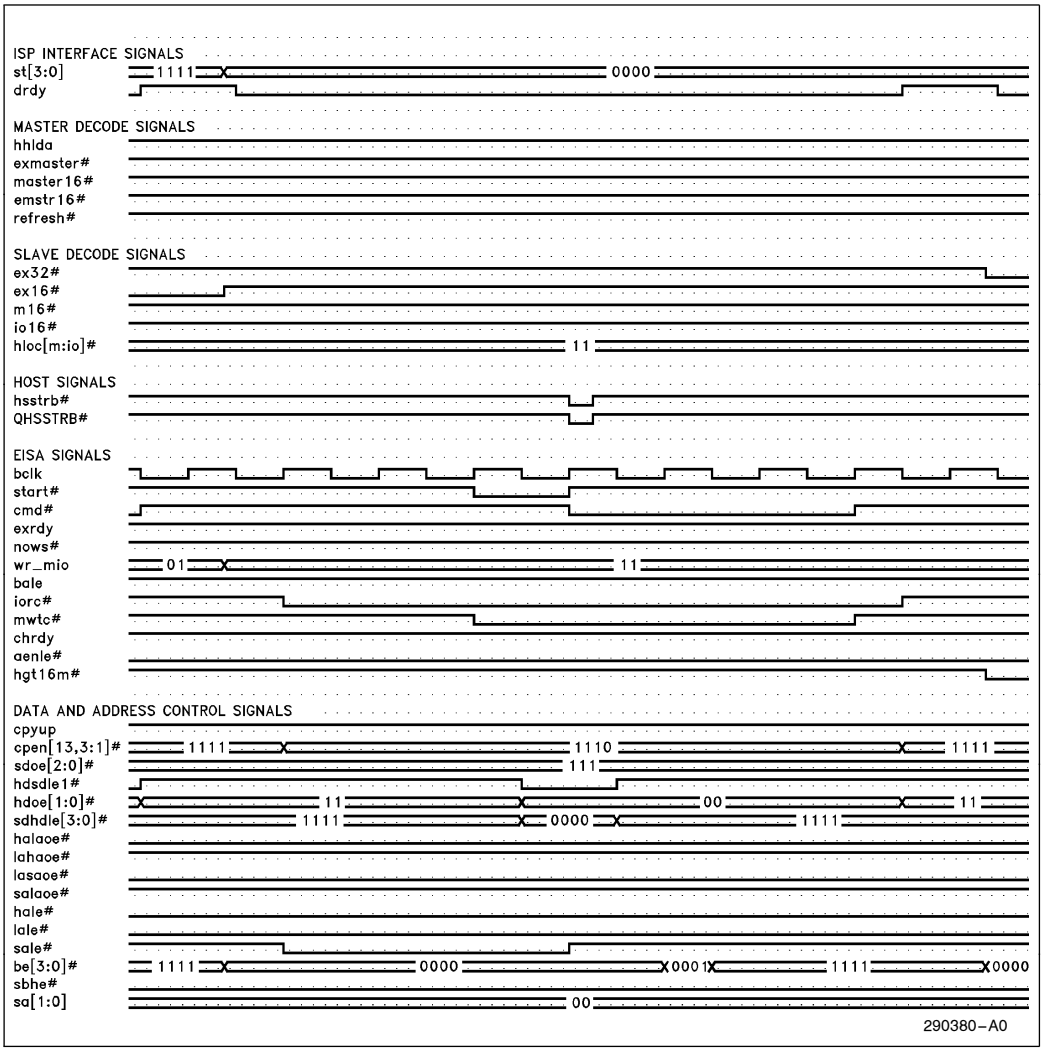
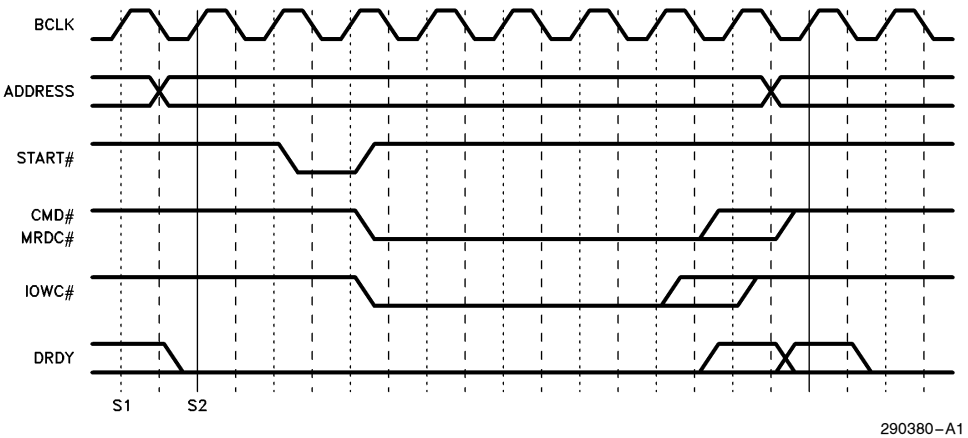
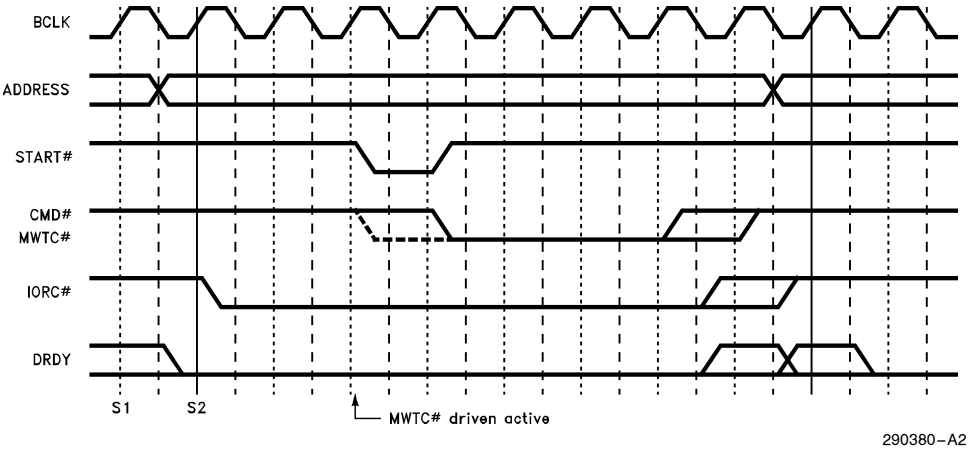


Figure 5-55. 8-Bit I/O to 8-Bit Memory Slave Compatible Cycle-One Byte Transfer



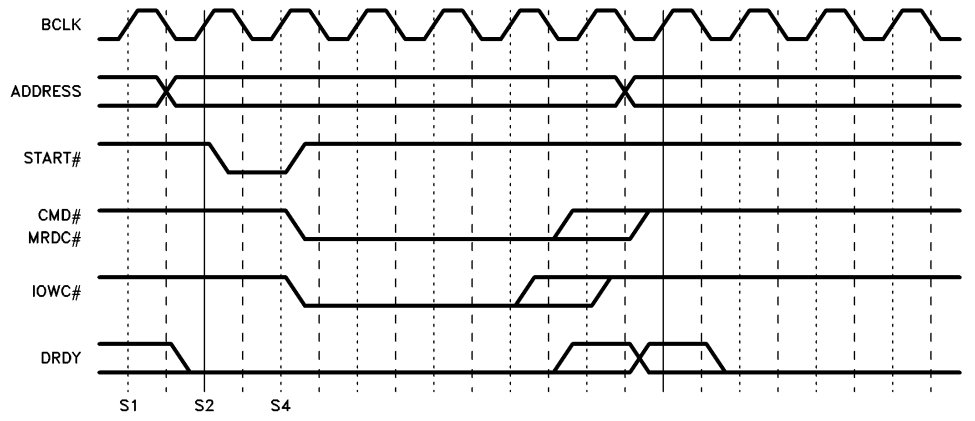
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]

Figure 5-56. Compatible DMA Read Cycle (Memory Size .GE. I/O Size)



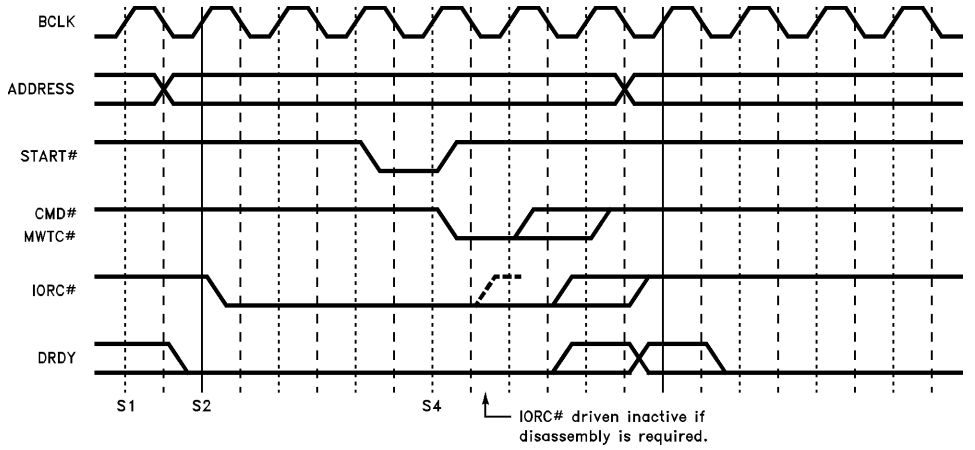
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]

Figure 5-57. Compatible DMA Write Cycle (Memory Size .GE. I/O Size)



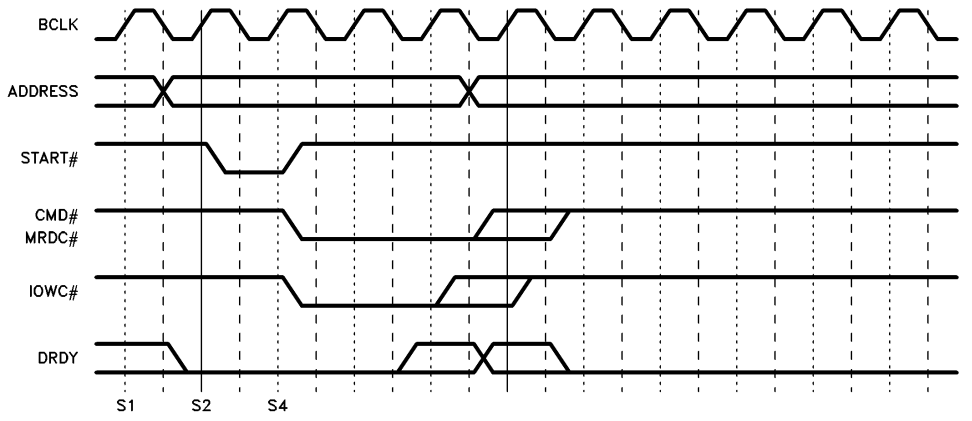
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S4—Sample EX32#, EX16#, M16#, HLOCMEM#

Figure 5-58. Type A DMA Read Cycle (Memory Size .GE. I/O Size)



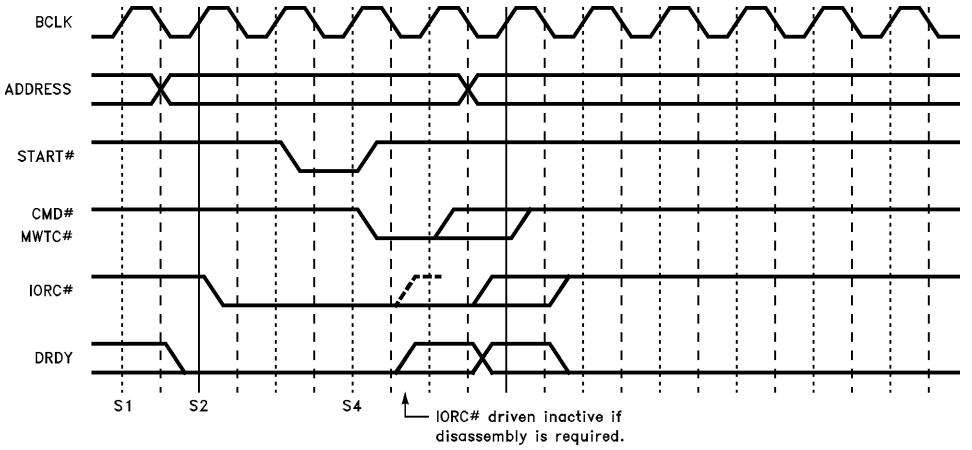
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S4—Sample EX32#, EX16#, M16#, HLOCMEM#

Figure 5-59. Type A DMA Write Cycle (Memory Size .GE. I/O Size)



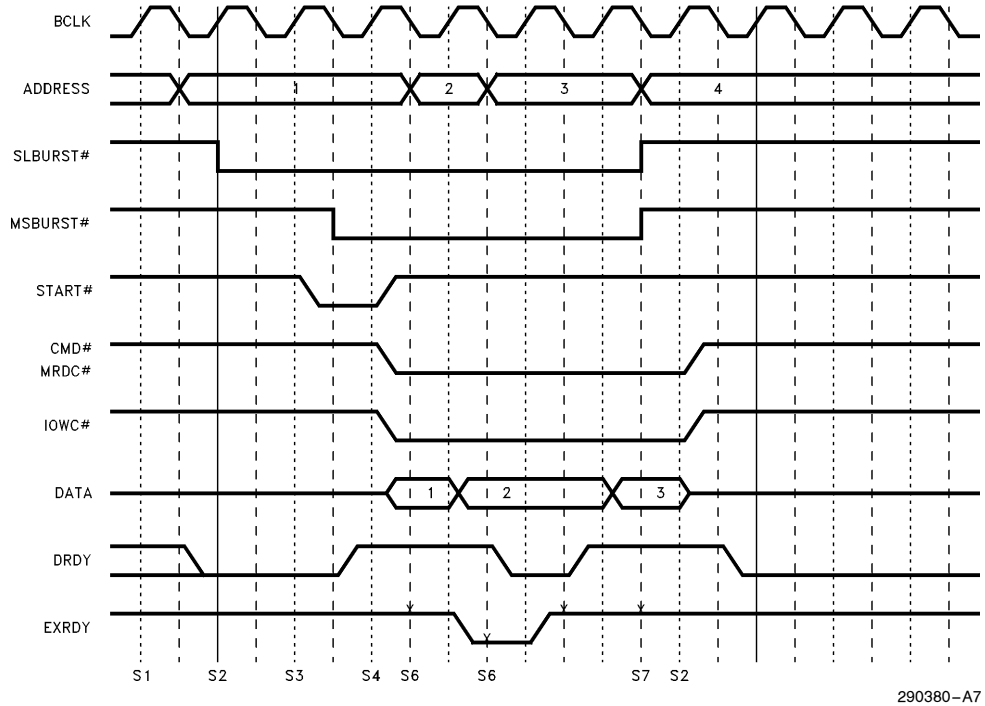
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S4—Sample EX32#, EX16#, M16#, HLOCMEM#

Figure 5-60. Type B DMA Read Cycle (Memory Size .GE. I/O Size)



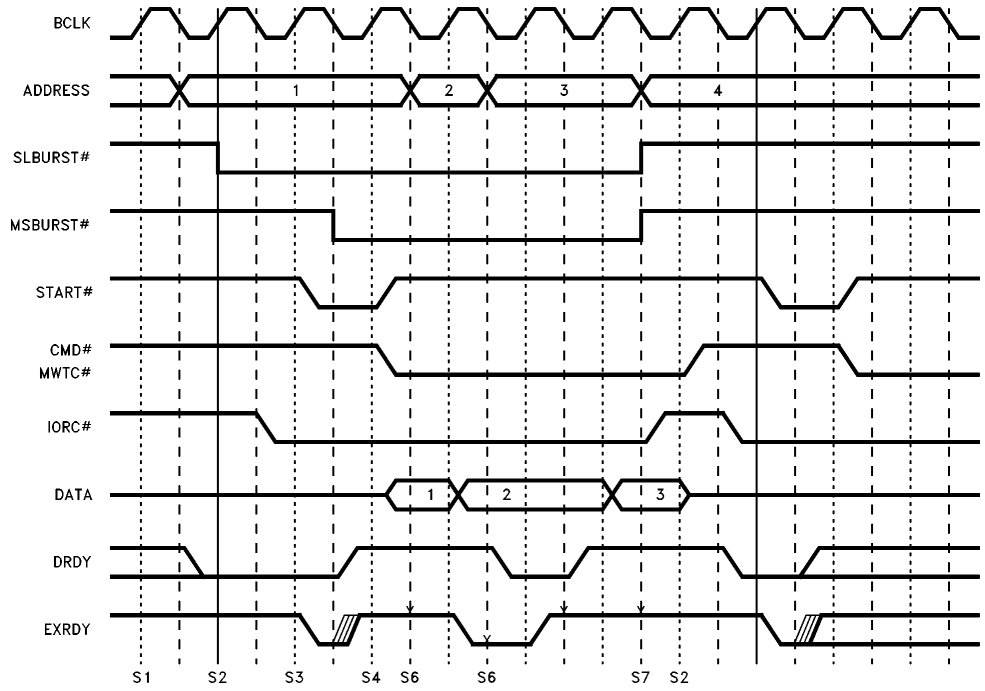
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S4—Sample EX32#, EX16#, M16#, HLOCMEM#

Figure 5-61. Type B DMA Write Cycle (Memory Size .GE. I/O Size)



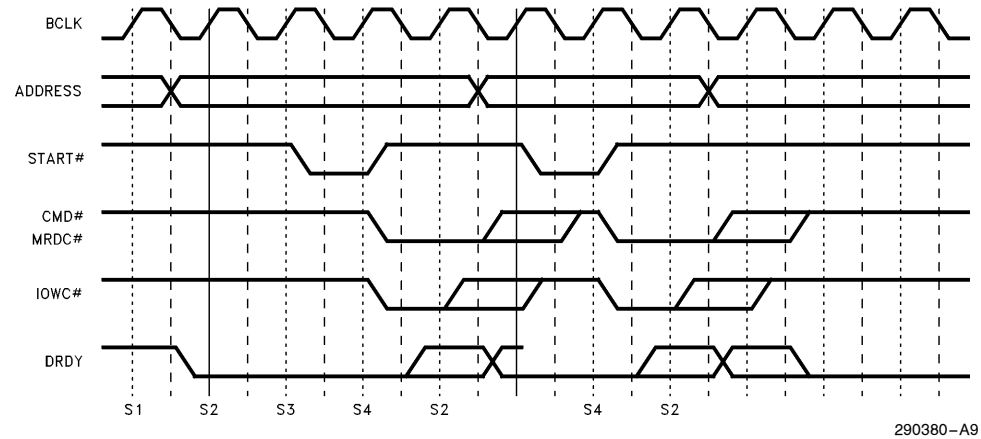
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S3—Sample SLBURST
S4—Sample EX32#, EX16#, M16#, HLOCMEM#
S6—No Change in status detected
S7—Change in status detected, (MSBURST#) deasserted
X = EBC sampling points

Figure 5-62. Burst DMA Read Cycle (Memory Size .GE. I/O Size)



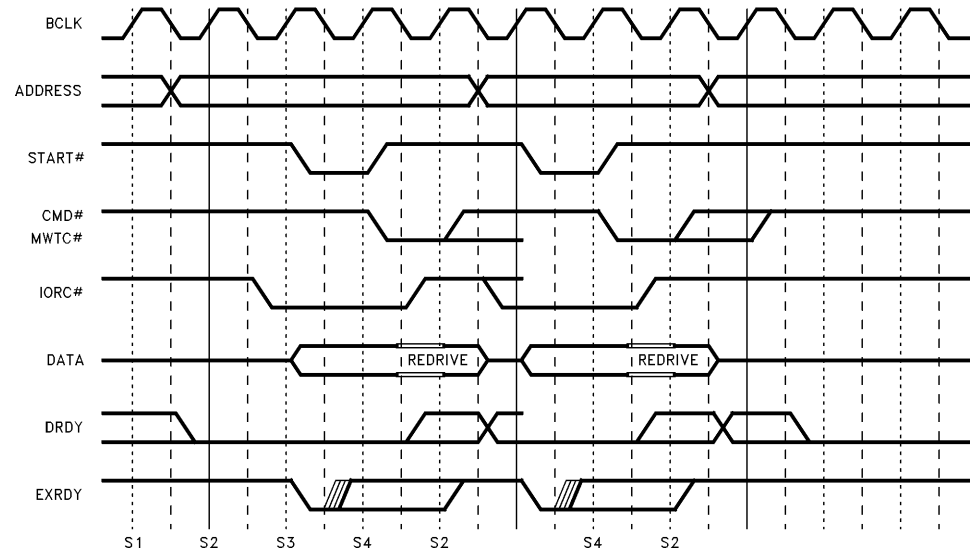
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S3—Sample SLBURST
S4—Sample EX32#, EX16#, M16#, HLOCMEM#
S6—No Change in status detected
S7—Change in status detected, (MSBURST#) deasserted
X = EBC sampling points

Figure 5-63. Burst DMA Write Cycle (Memory Size .GE. I/O Size)



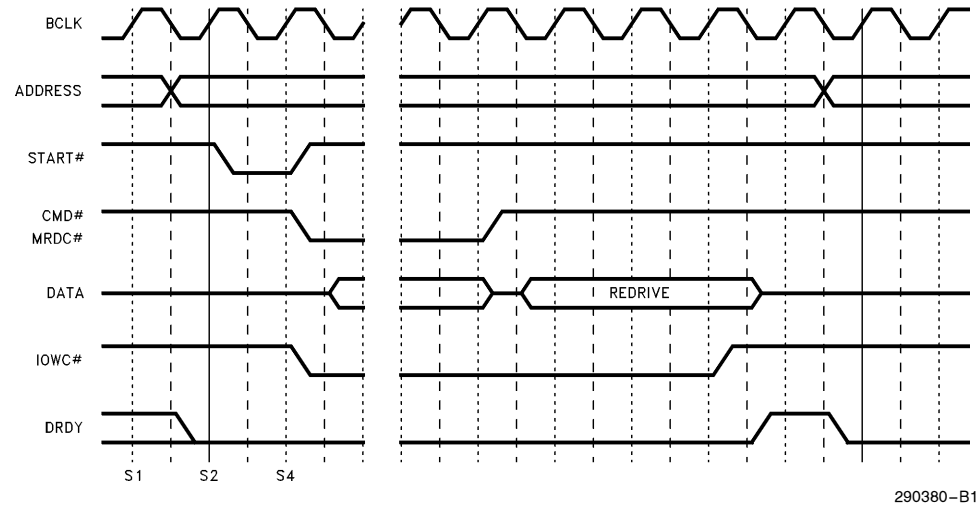
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S3—SLBURST sampled inactive, MSBURST# not asserted
S4—Sample EX32#, EX16#, M16#, HLOCMEM#

Figure 5-64. Burst DMA Read Cycle to Non-Burst Memory (Memory Size .GE. I/O Size)–Burst Backoff



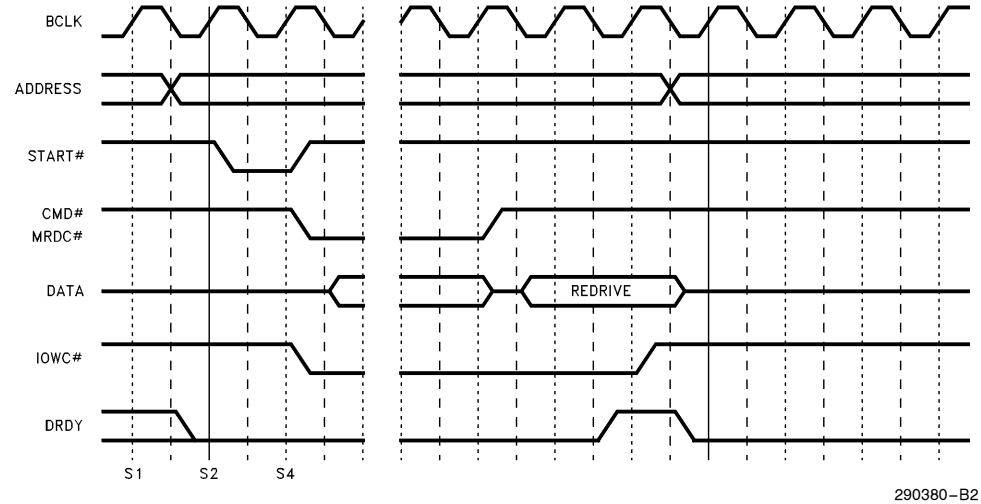
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S3—SLBURST sampled inactive, MSBURST# not asserted
S4—Sample EX32#, EX16#, M16#, HLOCMEM#

Figure 5-65. Burst DMA Write Cycle to Non-Burst Memory (Memory Size .GE. I/O Size) and (Memory Size .LT. I/O Size)–Burst Backoff and Redrive



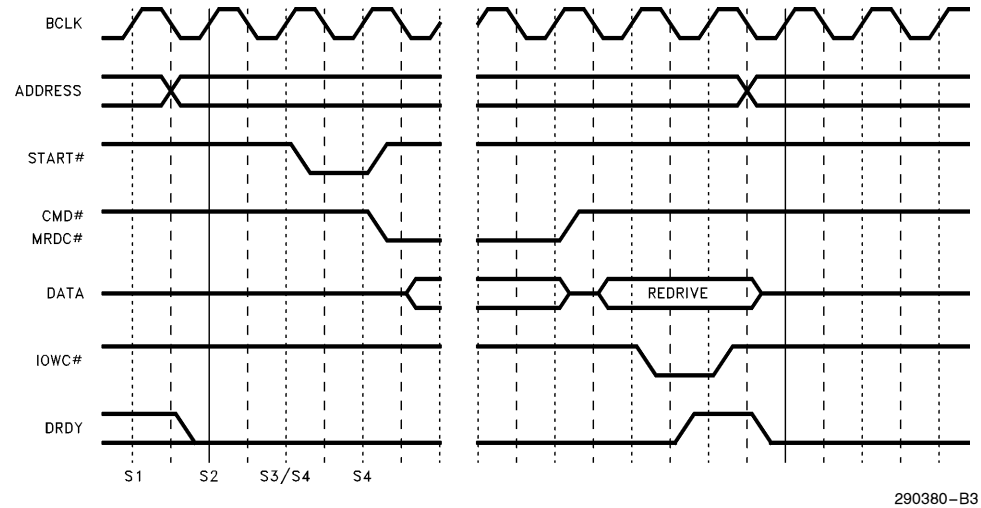
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S4—Sample EX32#, EX16#, M16#, HLOCMEM#

Figure 5-66. Type A DMA Read Cycle (Memory Size .LT. I/O Size)–Redrive



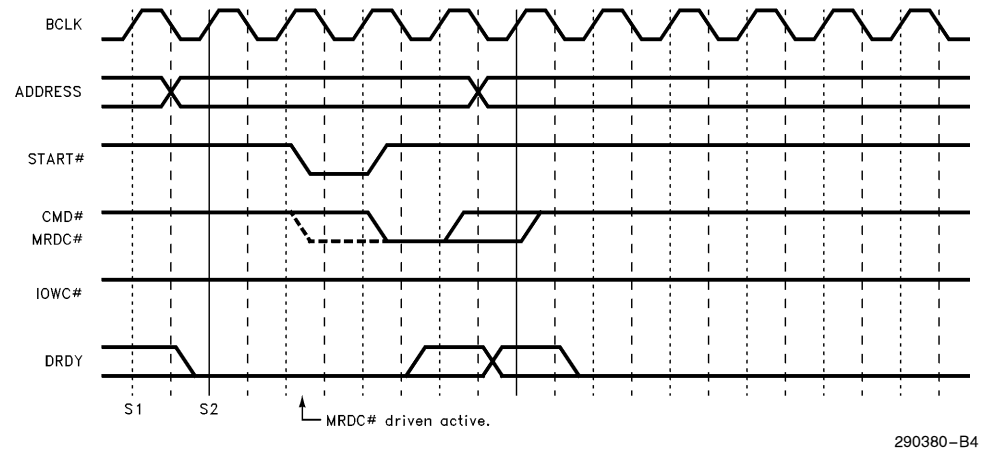
S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S4—Sample EX32#, EX16#, M16#, HLOCMEM#

Figure 5-67. Type B Read Cycle (Memory Size .LT. I/O Size)–Redrive



S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]
S3—Sample SLBURST
S4—Sample EX32#, EX16#, M16#, HLOCMEM# (Assembly Required detected)

Figure 5-68. Burst DMA Read with Assembly Required (Memory Size .LT. I/O Size)–Redrive



S1—Sample HHLDA, EXMASTER#, EMSTR16#, REFRESH#
S2—Sample ST[3:0]

Figure 5-69. Refresh Cycle

5.7 Miscellaneous Cycles

This section includes a halt/shutdown, SPWROK, and software reset (RSTAR#) cycle.

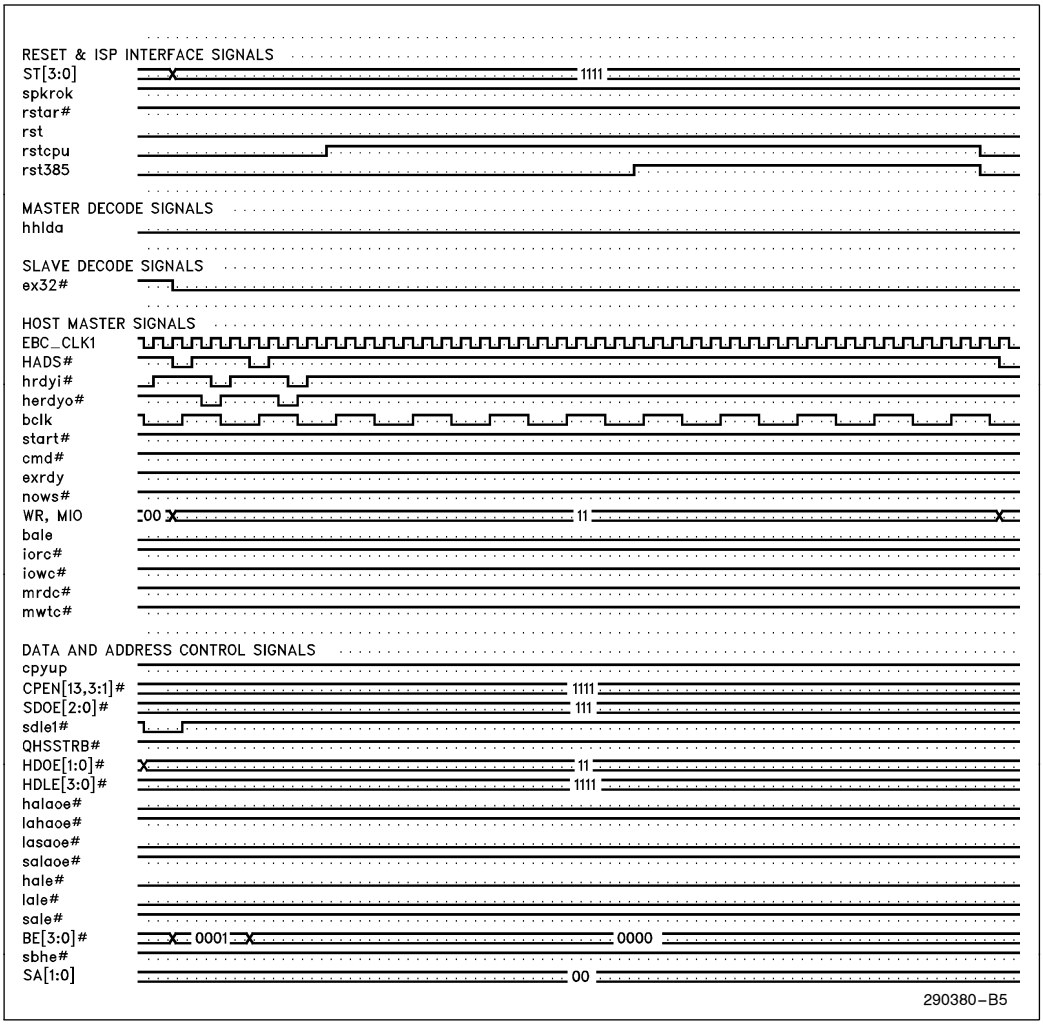


Figure 5-70. Halt, Flush, or Write Back Cycle followed by a Shutdown Cycle (82350 System Environment)

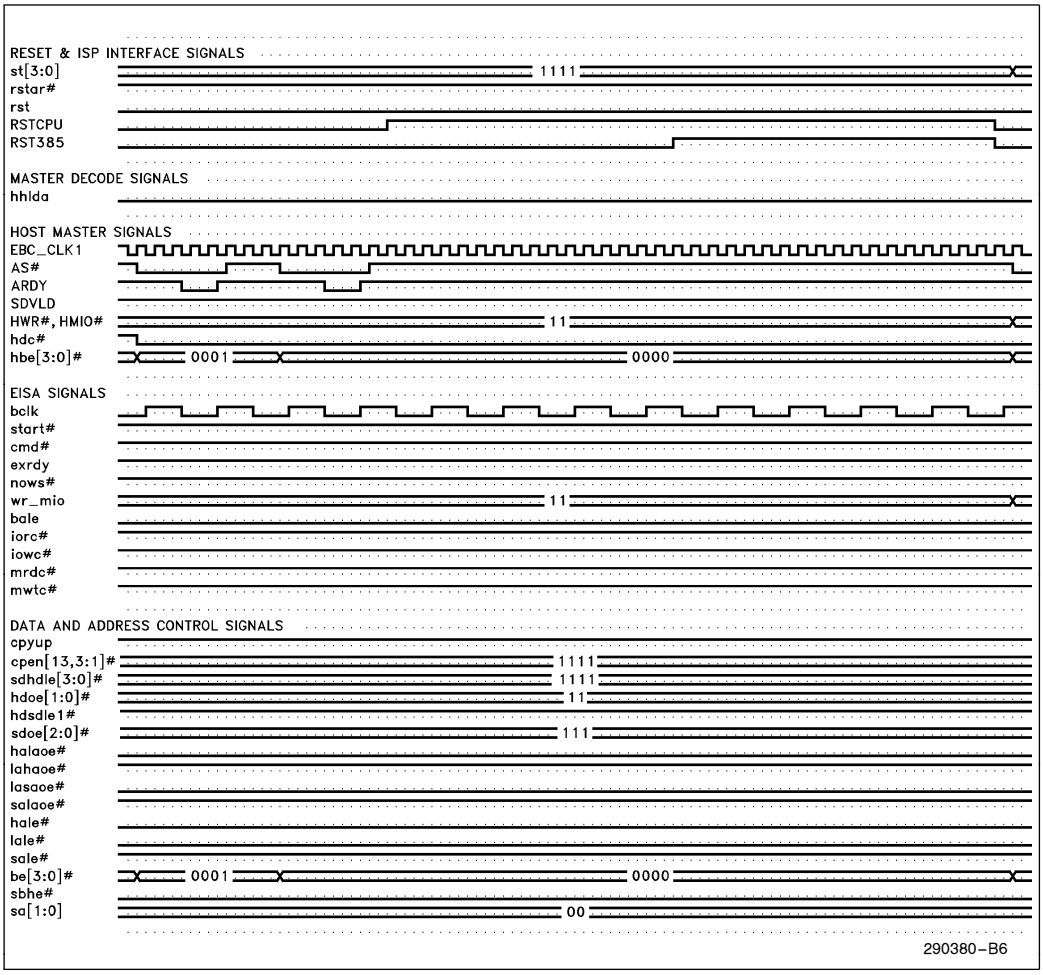


Figure 5-71. Halt, Flush, or Write Back Cycle followed by a Shutdown Cycle (82350DT System Environment)

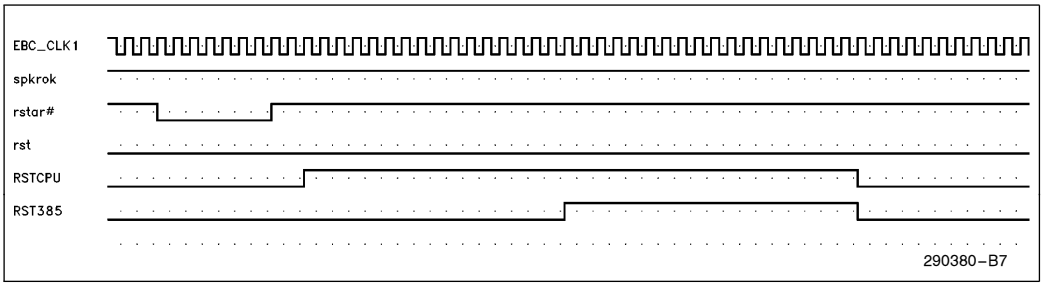


Figure 5-72. RSTAR#

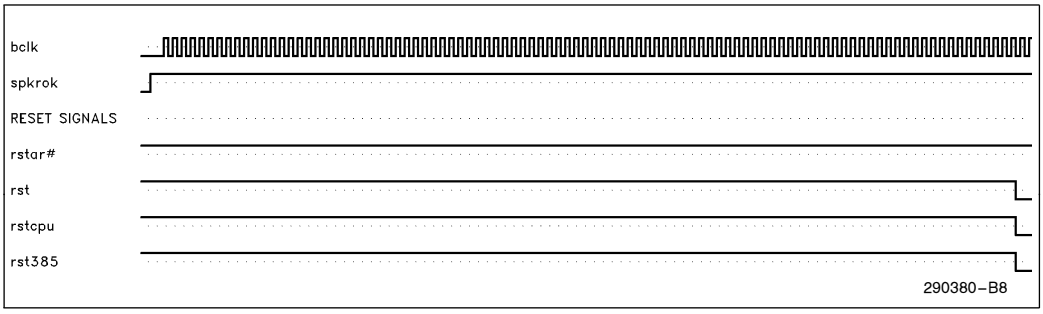


Figure 5-73. SPWROK

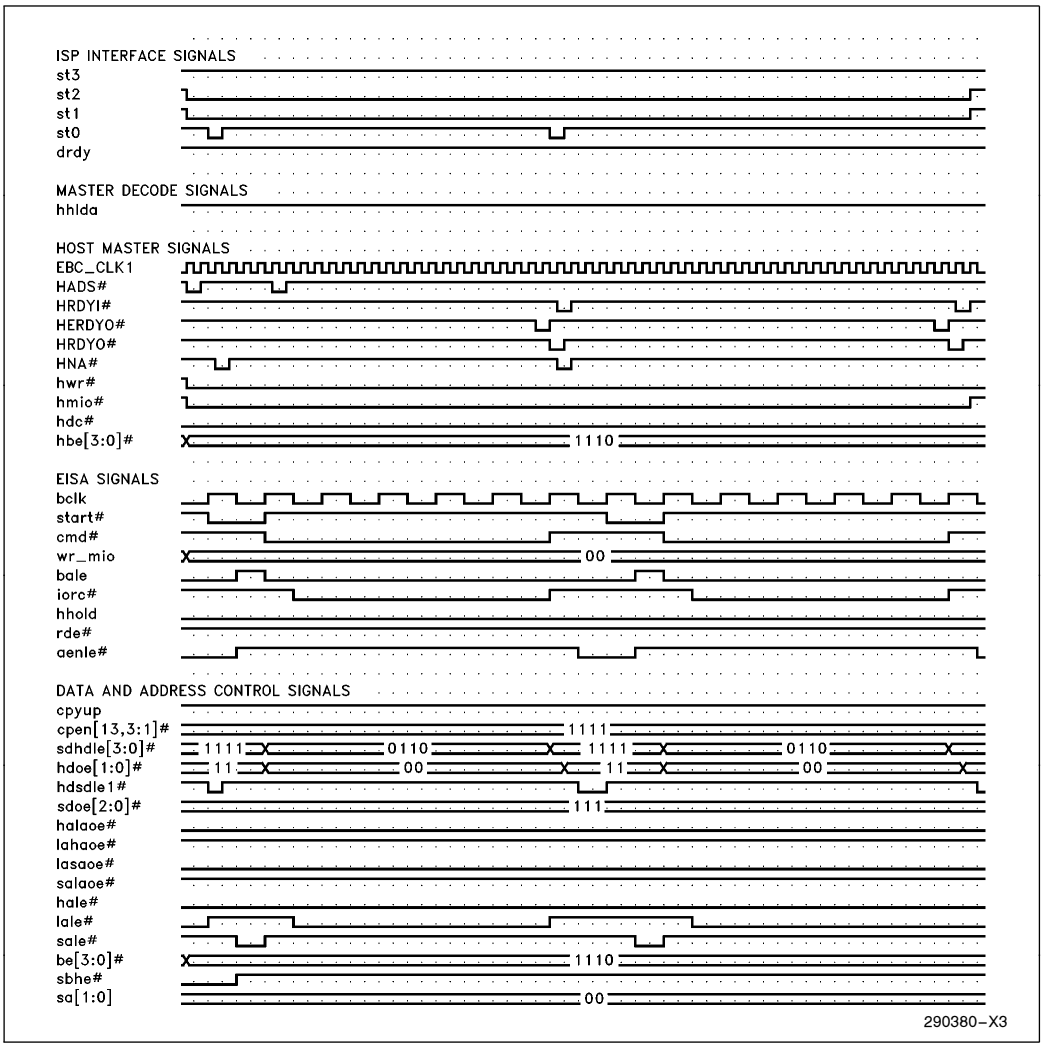


Figure 5-74. Interrupt Acknowledge Cycle (82350 System Environment)

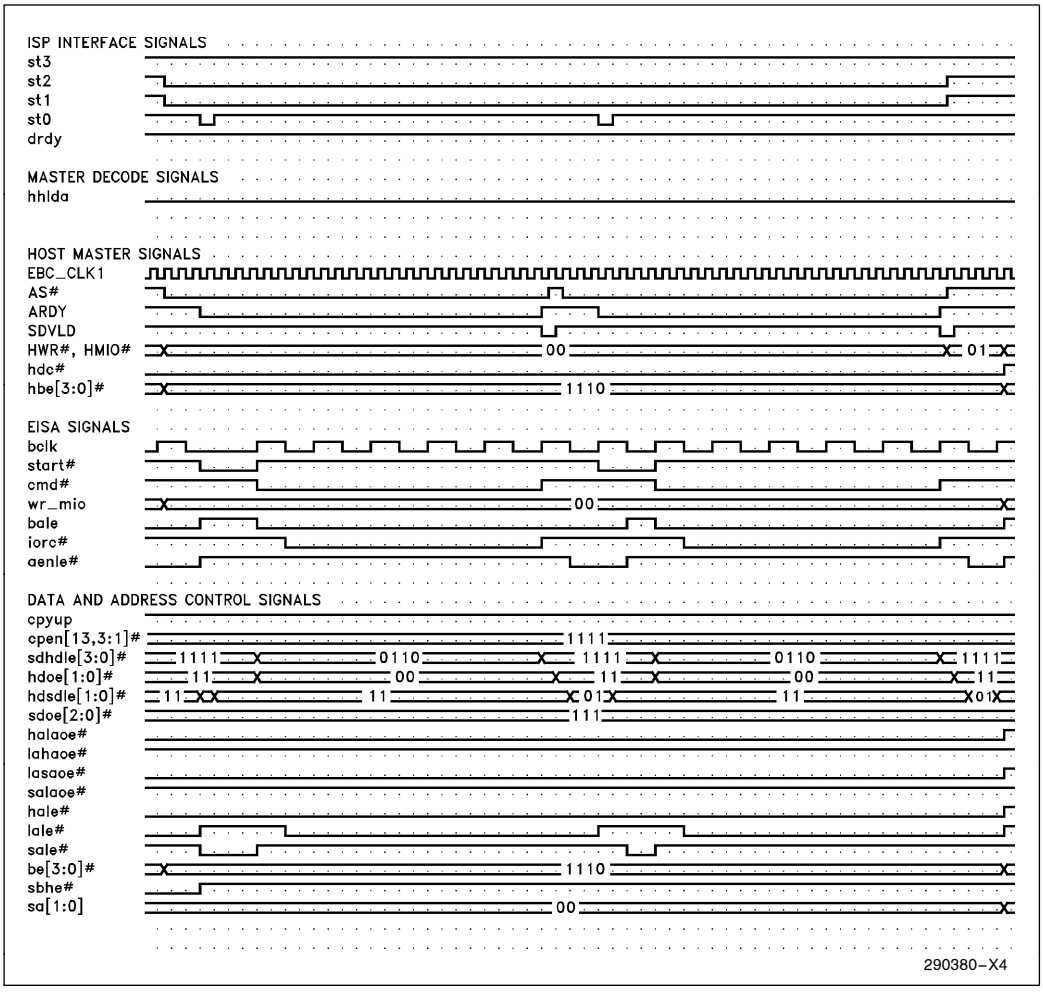


Figure 5-75. Interrupt Acknowledge Cycle (82350DT System Environment)

6.0 PIN AND PACKAGE INFORMATION

6.1 82358DT EISA Bus Controller Pinout Information

82358DT (132 PINS)

```
NAME = PIN NAME
TYPE = I-INPUT, O-OUTPUT, B-INPUT/OUTPUT, TS-TRI STATED
       BC-INPUT/OUTPUT OPEN COLLECTOR, NC-NO CONNECT, V-POWER
PIN    = PIN LOCATION
```

Name	Type	Pin	Description
Host Bus Signals (26 Pins)			
HCLKCPU	I	89	Host CPU Clock
HADS0#/AS#	I	72	Host Address Status/Address Strobe
HADS1#	I	128	Host Address Status
HBE3#	B, TS	118	Host Byte Enables
HBE[2:0]#	B, TS	120:122	Host Byte Enables
HNA#/SBMODE#	B, TS	106	Host Next Address/Strobed Bus Mode
HD/C#	B, TS	108	Host Data or Control Cycle
HM/IO#	B, TS	109	Host Memory or I/O
HW/R#	B, TS	110	Host Write or Read
HLOCMEM#	I	102	Host Local Memory
HLOCIO#	I	103	Host Local IO
HSTRETCH#	I	104	Host Cycle Stretch
HRDYI#	I	127	Host Bus Ready Input
HRDYO#/SDVLD	O, TS	112	Host Bus Ready Output/System Data Valid
HERDYO#/ARDY	O	114	Host Bus Early Ready Output/System Async Ready
HHOLD	O	115	Host Hold Request
HHLDA	I	129	Host Hold Acknowledge
HLOCK#	I	130	Host Bus Lock
HSSTRB#	O	116	Host Snoop Strobe
QHSSTRB#	O	19	i486 CPU Snoop Strobe
HKEN#	I	126	Host Cache Enable
HGT16M#	I	131	Host Greater Than 16 Megabytes Being Accessed
PWEN#	I	123	Posted Write Enable
AMODE	I	124	Address/Status Buffer Control
EISA Signals (14 Pins)			
BE[3:0]#	B, TS	60:63	Bytes Enables
M-IO	B, TS	73	Memory or I/O Cycle
W-R	B, TS	64	Write or Read Cycle
START#	B, TS	31	Start of EISA Cycle
CMD#	O	41	EISA Command
MSBURST#	B, TS	58	Master Burst
SLBURST#	I	57	Slave Burst
EX32#	BC	56	EISA 32-Bit Slave Size
EX16#	BC	55	EISA 16-Bit Slave Size
EXRDY	BC	53	EISA Ready
LOCK#	O, TS	36	Locked Cycle

6.1 82358DT EISA Bus Controller Pinout Information (Continued)

Name	Type	Pin	Description
ISA Signals (17 Pins)			
BALE	O	39	Bus Address Latch Enable
MASTER16#	I	66	16-Bit Master (EISA or ISA)
BCLKOUT	O	86	EISA/ISA Bus Clock Output
IORC#	B, TS	52	I/O Read Control Strobe
IOWC#	B, TS	50	I/O Write Control Strobe
IO16#	BC	49	16-Bit I/O Slave Size
MRDC#	B, TS	48	Memory Read Control Strobe
MWTC#	B, TS	47	Memory Write Control Strobe
M16#	I	46	16-Bit Memory Slave Size
SMRDC#	O, TS	38	Standard Memory Read Control Strobe (Under 1 Meg)
SMWTC#	O, TS	37	Standard Memory Write Control Strobe (Under 1 Meg)
CHRDY	BC	65	Channel Ready
NOWS#	I	32	Zero Wait States
SA[1:0]	B, TS	44,43	System A1 & A0
SBHE#	B, TS	42	System Byte High Enable
REFRESH#	I	33	Refresh Cycle
ISP Signals (9 Pins)			
DHOLD	I	105	ISP Hold Request
DRDY	B, TS	77	ISP Ready
GT1M#	I	71	Greater than 1 Megabyte
ST[3:0]	B, TS	82:79	DMA Status (8,16,32-Bit Device & Type A,B,Burst(C) & Compatible Timings)
EXMASTER#	I	70	EISA Master
EMSTR16#	I	69	Early Indication of 16-Bit ISA Master
Data Buffer Control (All Signals are Outputs) (16 Pins)			
SDCPYEN01#	O	4	Copy Enable Between Bytes 0 and 1
SDCPYEN02#	O	5	Copy Enable Between Bytes 0 and 2
SDCPYEN03#	O	6	Copy Enable Between Bytes 0 and 3
SDCPYEN13#	O	7	Copy Enable Between Bytes 1 and 3
SDCPYUP	O	8	Copy Up (Low Byte to High Byte)
SDHDLE[3:0]#	O	10:13	System (EISA) Data to Host Data Latch Enables
SDOE[2:0]#	O	14,16,17	System (EISA) Data Output Enables
HDSDLE1#	O	18	Host Data to (EISA) Data Latch Enables
HDOE[1:0]#	O	20,22	Host Data Output Enable
Address Buffer Control (7 Pins)			
HALAOE#	O	23	Host Address to EISA LA Output Enable
HALE#	O	24	Host Address Latch Enable
LASAOE#	O	25	EISA LA to EISA SA Output Enable
LAHAOE#	O	26	EISA LA to Host Address Output Enable
LALE#	O	28	LA Latch Enable
SALAOE#	O	29	EISA SA to EISA LA Output Enable
SALE#	O	30	SA Latch Enable
Reset Signals (5 Pins)			
SPWROK	I	101	Synchronous Power OK
RST	O	90	System Reset
RSTAR#	I	98	Restart
RSTCPU	O	93	Reset CPU Only
RST385	O	91	Reset 385 Only

6.1 82358DT EISA Bus Controller Pinout Information (Continued)

Name	Type	Pin	Description
Configuration Signals (5 Pins)			
CPU[3:0]	I	97:94	CPU Type and Frequency Indicator
RDE#	I	111	1 CLK1 Delay for Host to EISA Reads
Miscellaneous Signals (5 Pins)			
CLKKB	O	75	Keyboard Controller Clock
LIOWAIT#	I	3	Long Wait Between I/O Cycles
AENLE#	O	76	AEN Latch Enable
TEST1#	I	2	Tri-State All Outputs of the EBC
BCLKIN	I	83	BCLK Input for Synchronization
VCC & GND Signals (29 Pins)			
VCC	V		9,15,21,34,40,54,67,74,85,87,92,99,107,119,132
VSS	V		1,27,35,45,51,59,68,78,84,88,100,113,117,125
Total of 103 Control Pins and 29 Power Pins			

6.2 82358DT (EBC) Device Pin List

Device Pinout—132 Lead PQFP

Pin	Name	Type
1	V_{SS}	V
2	TEST 1#	I
3	LIOWAIT#	I
4	SDCPYEN01#	O
5	SDCPYEN02#	O
6	SDCPYEN03#	O
7	SDCPYEN13#	O
8	SDCPYUP	O
9	V_{CC}	V
10	SDHDLE3#	O
11	SDHDLE2#	O
12	SDHDLE1#	O
13	SDHDLE0#	O
14	SDOE2#	O
15	V_{CC}	V
16	SDOE1#	O
17	SDOE0#	O
18	HDSDLE1#	O
19	QHSSTRB#	O
20	HDOE1#	O
21	V_{CC}	V
22	HDOE0#	O
23	HALAOE#	O
24	HALE#	O
25	LASAOE#	O
26	LAHAOE#	O
27	V_{SS}	V
28	LALE#	O
29	SALAOE#	O
30	SALE#	O
31	START#	I/O, TS
32	NOWS#	I
33	REFRESH#	I
34	V_{CC}	V
35	V_{SS}	V
36	LOCK#	O, TS
37	SMWTC#	O, TS
38	SMRDC#	O, TS
39	BALE	O
40	V_{CC}	V
41	CMD#	O
42	SBHE#	I/O, TS
43	SA0	I/O, TS
44	SA1	I/O, TS

Pin	Name	Type
45	V_{SS}	V
46	M16#	I
47	MWTC#	I/O, TS
48	MRDC#	I/O, TS
49	IO16#	I/O, OC
50	IOWC#	I/O, TS
51	V_{SS}	V
52	IORC#	I/O, TS
53	EXRDY	I/O, OC
54	V_{CC}	V
55	EX16#	I/O, OC
56	EX32#	I/O, OC
57	SLBURST#	I
58	MSBURST#	I/O, TS
59	V_{SS}	V
60	BE0#	I/O, TS
61	BE1#	I/O, TS
62	BE2#	I/O, TS
63	BE3#	I/O, TS
64	W-R	I/O, TS
65	CHRDY	I/O, OC
66	MASTER16#	I
67	V_{CC}	V
68	V_{SS}	V
69	EMSTR16#	I
70	EXMASTER#	I
71	GTIM#	I
72	HADS0#/AS#	I
73	M-IO	I/O, TS
74	V_{CC}	V
75	CLKKB	O
76	AENLE#	O
77	DRDY	I/O, TS
78	V_{SS}	V
79	ST0	I/O, TS
80	ST1	I/O, TS
81	ST2	I/O, TS
82	ST3	I/O, TS
83	BCLKIN	I
84	V_{SS}	V
85	V_{CC}	V
86	BCLKOUT	O
87	V_{CC}	V
88	V_{SS}	V

Pin	Name	Type
89	HCLKCPU	I
90	RST	O
91	RST385	O
92	V_{CC}	V
93	RSTCPU	O
94	CPU0	I
95	CPU1	I
96	CPU2	I
97	CPU3	I
98	RSTAR#	I
99	V_{CC}	V
100	V_{SS}	V
101	SPWROK	I
102	HLOCMEM#	I
103	HLOCIO#	I
104	HSTRETCH#	I
105	DHOLD	I
106	HNA#/SBMODE#	I/O, TS
107	V_{CC}	V
108	HD/C#	I/O, TS
109	HM/IO#	I/O, TS
110	HW/R#	I/O, TS
111	RDE#	I
112	HRDYO#/SDVLD	O, TS
113	V_{SS}	V
114	HERDYO#/ARDY	O
115	HHOLD	O
116	HSSTRB#	O
117	V_{SS}	V
118	HBE3#	I/O, TS
119	V_{CC}	V
120	HBE2#	I/O, TS
121	HBE1#	I/O, TS
122	HBE0#	I/O, TS
123	PWEN#	I
124	AMODE	I
125	V_{SS}	V
126	HKEN#	I
127	HRDYI#	I
128	HADS1#	I
129	HHLDA	I
130	HLOCK#	I
131	HGT16M#	I
132	V_{CC}	V

6.3 82358DT Pin Diagram

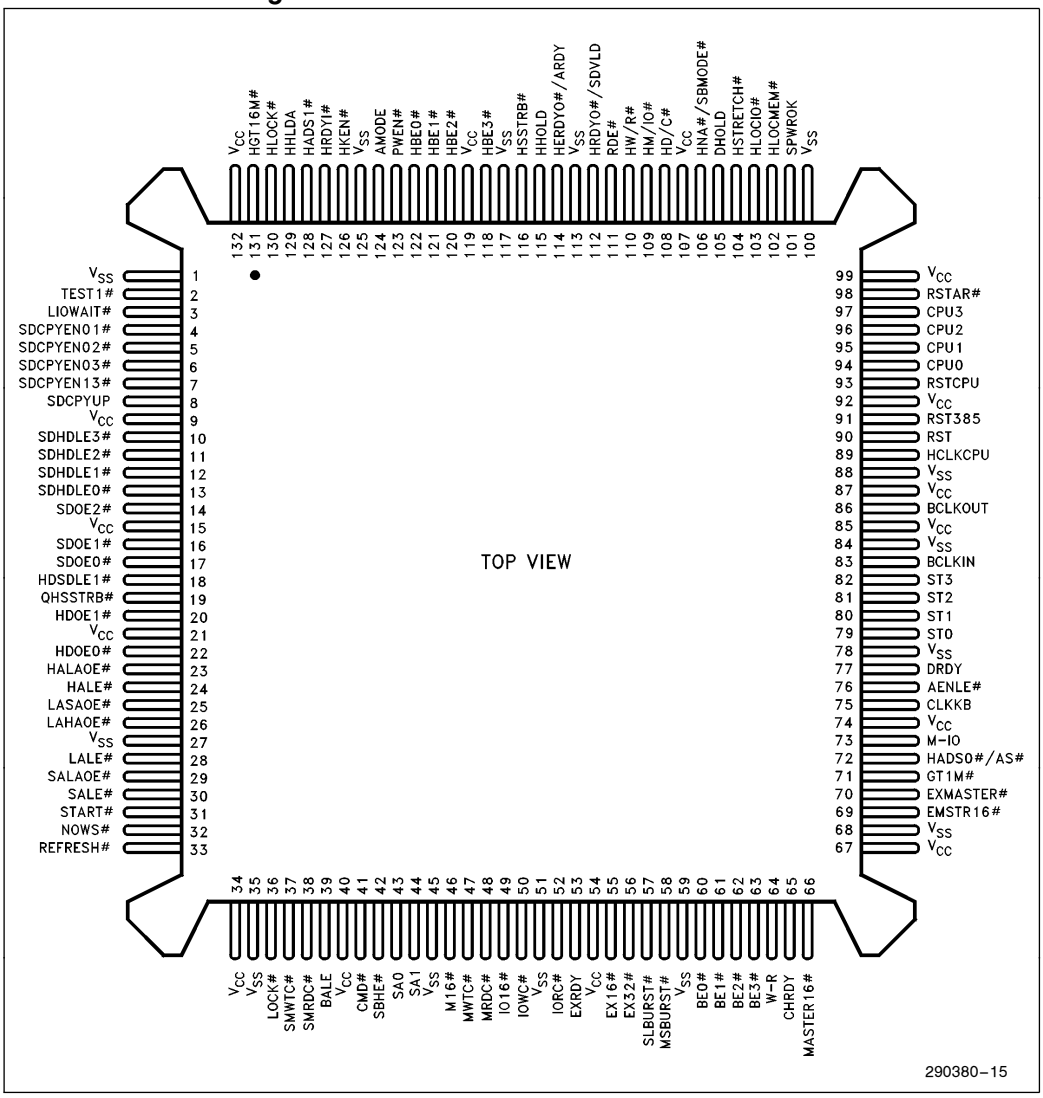


Figure 6-1. 82358DT Pin Diagram

6.4 82358DT Thermal Specification

The 82358DT is specified for operation when the case temperature is within the range of 0°C—85°C. The case temperature may be measured in any environment, to determine whether the device is within the specified operating range.

The PQFP case temperature should be measured at the center of the top surface opposite the pins, as shown in Figure 6-2 below.

Process Name: CHMOSIV

Temperature Rise Vs. Time:

Time (sec)	Temperature Rise Unit Power (c/w)
0	0
1	3.7
2	6.0
3	7.3
5	9.5

6.5 82358DT Packaging Information

(See Packaging Specification Order No. 231369)

INTRODUCTION

The 82358DT comes in a JEDEC standard Gull wing package (25 Mil pitch), with ''bumpers'' on the corners for ease of handling. Please refer to the accompanying table for the package specifications for pinouts.

NOTE:
Individual pinouts are numbered consistently with the numbering scheme depicted in the accompanying figures.

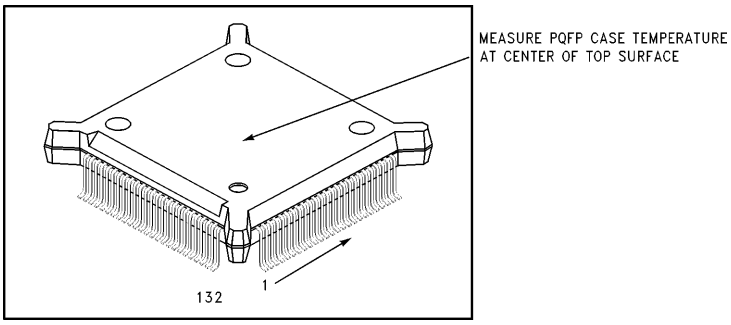


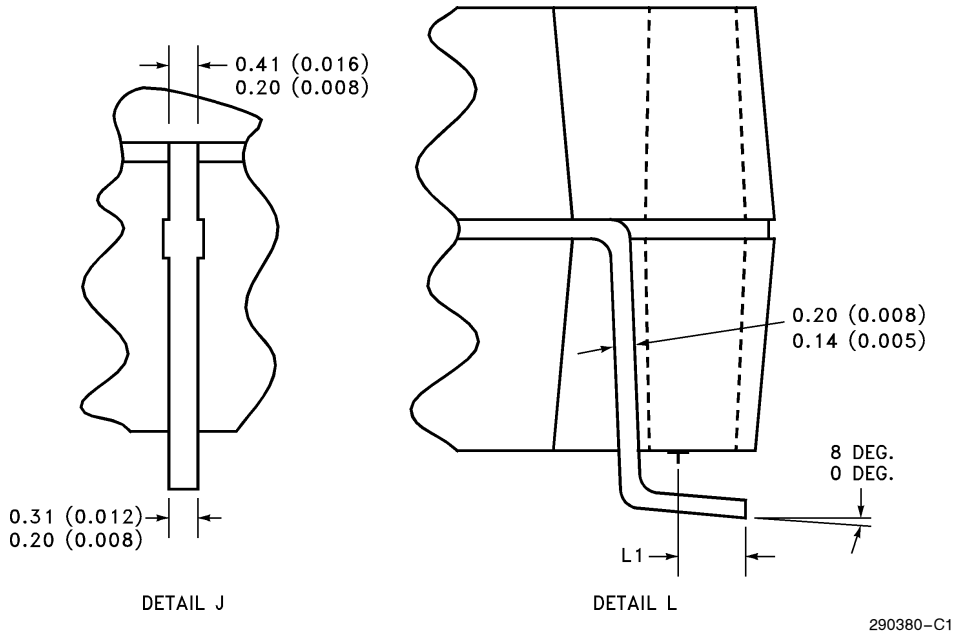
Figure 6-2. Plastic Quad Flat Pack (PQFP)

Table 6-1. 82358DT PQFP Package Thermal Characteristics

Thermal Resistance - °C/Watt					
Parameter	Air Flow Rate (Ft/Min)				
	0	200	400	600	800
θ Junction - Case	7	7	7	7	7
θ Case to Ambient	22	17.5	14.5	12	10

NOTES:
1. Table 6-1 applies to the 82358DT PQFP plugged into a socket or soldered directly on to the board.
2. $O_{JA} = O_{JC} + O_{CA}$

Case Outline Drawings
Plastic Fine Pitch Chip Carrier
0.84 mm Pitch



mm (inch)

Figure 6-3. Typical Lead

Symbol	Description	Min	Max	Min	Max
N	Lead Count	132		132	
A	Package Height	0.160	0.170	4.06	4.32
A1	Standoff	0.020	0.030	0.51	0.76
D, E	Terminal Dimension	1.075	1.085	27.31	27.56
D1, E1	Package Body	0.947	0.953	24.05	24.21
D2, E2	Bumper Distance	1.097	1.103	27.86	28.02
D3, E3	Lead Dimension	0.800 Ref		20.32 Ref	
L1	Foot Length	0.020	0.030	0.51	0.76
		Inch		mm	

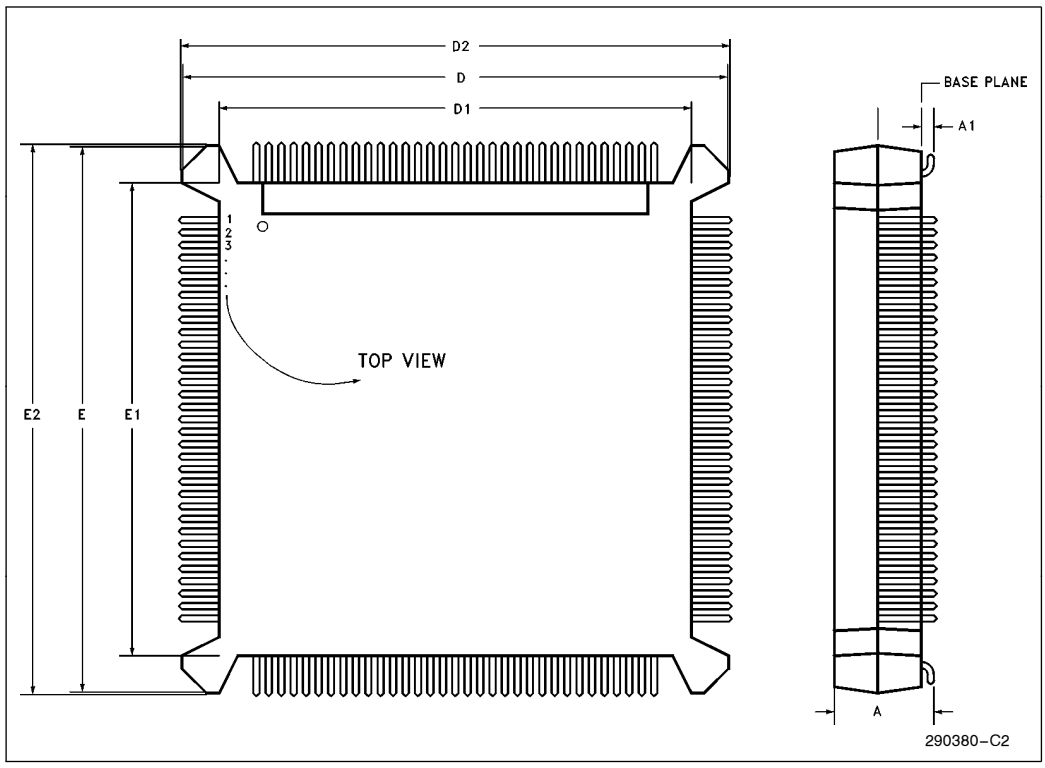


Figure 6-4. Principal Dimensions and Datums

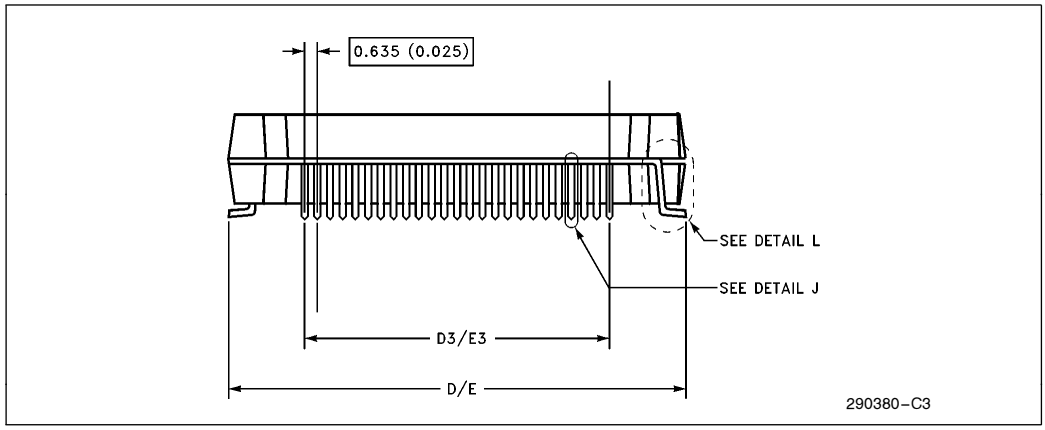


Figure 6-5. Terminal Details

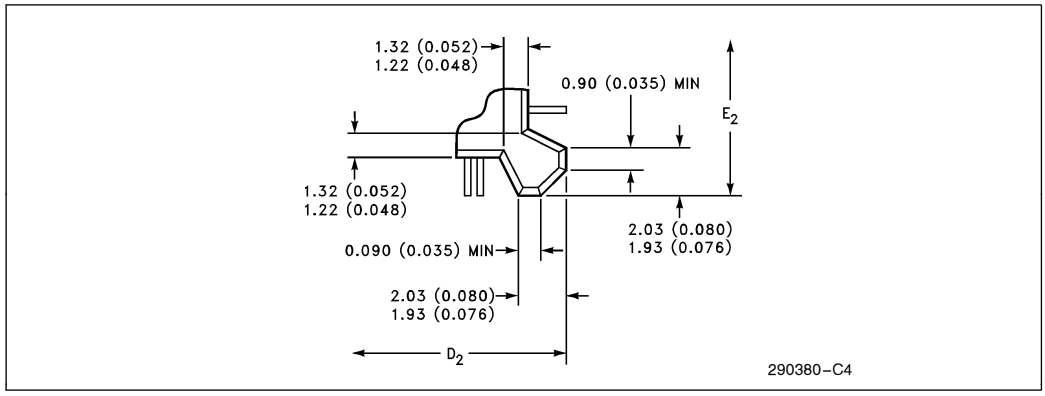


Figure 6-6. Bumper Detail

7.0 D.C. SPECIFICATIONS

7.1 Maximum Ratings

Case Temperature Under Bias	−65°C to +110°C
Storage Temperature	−65°C to +150°C
Supply Voltages with Respect to Ground	−0.5V to V_{CC} + 0.5V
Voltage on Any Pin	−0.5V to V_{CC} + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

7.2 D.C. Specification Table

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C; T_A = 0°C to +70°C

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH1} V_{IH2} V_{IH3}	Input High Voltage Input High Voltage BCLKIN Input High Voltage	2.0 3.7 V_{CC} − 2.1	V_{CC} + 0.5 V_{CC} + 0.5 V_{CC} + 0.5	V V V	(Note 5) (Note 6)
V_{OLC} V_{OHC}	BCLK Output Low BCLK Output High	 V_{CC} − 0.5	0.4	V V	I_{OL} = 24 mA I_{OH} = −4 mA
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	 2.4	0.45	V V	I_{OL} = 5 mA(3) I_{OH} = −1 mA(3)
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	 2.4	0.45	V V	I_{OL} = 24 mA(2) I_{OH} = −4 mA(2)
V_{OL3} V_{OH3}	Output Low Voltage Output High Voltage	 2.4	0.45	V V	I_{OL} = 5 mA(1) I_{OH} = −250 μA(1)
I_{LI1} I_{LI2}	Input Leakage Input Leakage	 −45	±15 −1000	μA μA	0V < V_{IN} < V_{CC} V_{IN} = 2.4V(7)
I_{LO}	Output Leakage		±15	μA	0.45 < V_{IN} < V_{CC}
I_{CC}	V_{CC} Supply Current		200	mA	HCLK = 66 MHz(8)

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
$C_{I/O}$	I/O Capacitance		12	16	pF	@ 1 MHz(4)
C_{IN}	Input Capacitance		7.5	11	pF	@ 1 MHz(4)

NOTES:

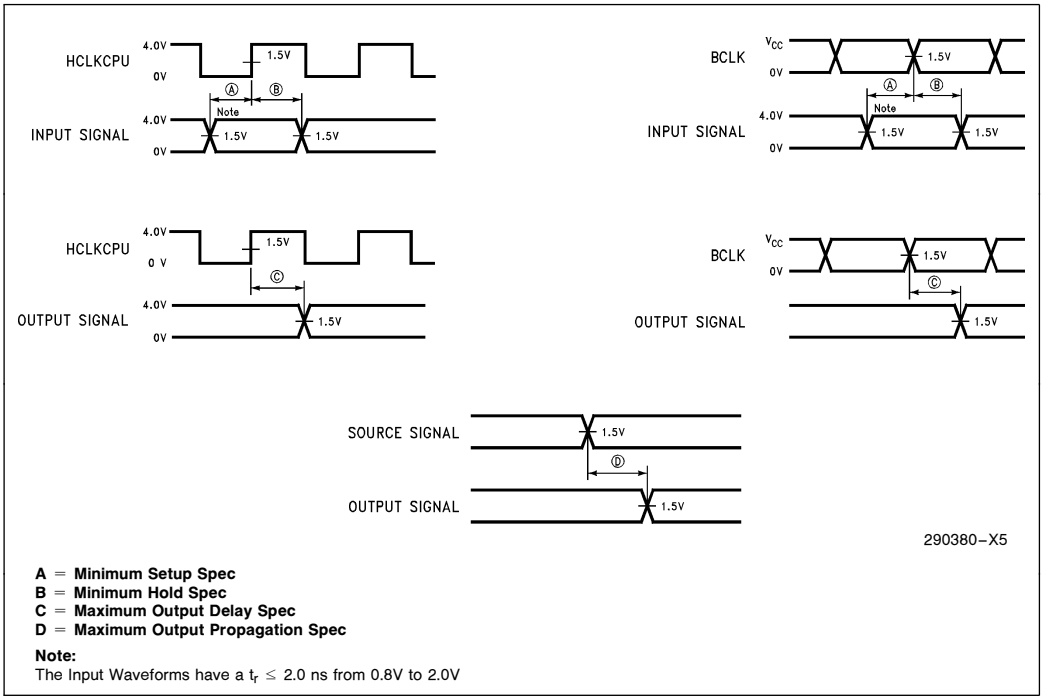
1. V_{OL3} and V_{OH3} apply only to signals that do not drive onto buses in the system. These are: DRDY, ST[3:0], SDCPYENx#, SDCPYUP, SDHDLE[3:0]#, SDOE[2:0]#, HDSDLE1#, HDOE[1:0]#, HALAOE#, HALE#, LASAOE#, LAHAOE#, LALE#, SALAOE#, SALE#, RSTCPU, RST385, CLKKB, AENLE#.
2. V_{OL2} and V_{OH2} apply only to the signals that directly drive the EISA bus and are not slot specific. These are: BE[3:0]#, M-IO, W-R, START#, CMD#, MSBURST#, EX32#, EX16#, EXRDY, LOCK#, BALE, IORC#, IOWC#, IO16#, MRDC#, MWTC#, SMRDC#, SMWTC#, CHRDY, SA[1:0], SBHE#.
3. V_{OL1} and V_{OH1} apply to all other outputs. These are: HNA#/SBMODE#, HD/C#, HM/IO#, HW/R#, HBE[3:0]#, HRDYO#/SDVLD, HERDYO#/ARDY, HHOLD, HSSTRB#, QHSSTRB#, RST.
4. Sampled only.
5. V_{IH1} applies to all signals, except HCLKCPU in 386 CPU mode.
6. V_{IH2} applies only to HCLKCPU in 386 CPU mode.
7. I_{LI2} applies to HALE#, HNA#/SBMODE, HBE1#, and HBE0# only.
8. Tested with loads. Typical no loads value = 50 mA. Typical with loads value = 95 mA.

8.0 A.C. SPECIFICATIONS

In the following A.C. Specification section, the specifications and diagrams refer to both the 386 and i486 microprocessors, and the 82350 and 82350DT systems, unless otherwise stated.

The A.C. specifications given in the following tables consist of output delays, input setup requirements, input hold requirements, and propagation delays.

A.C. specification measurements are defined in Figure 8-1. Input levels must be driven to the voltage levels indicated in Figure 8-1, when A.C. specifications are measured. The output capacitive test loads are shown in Section 8.2. 82358DT output delays are specified with minimum and maximum limits, measured as shown. 82358DT input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct 82358DT operation.



A = Minimum Setup Spec
B = Minimum Hold Spec
C = Maximum Output Delay Spec
D = Maximum Output Propagation Spec

Note:
The Input Waveforms have a $t_r \leq 2.0$ ns from 0.8V to 2.0V

Figure 8-1. A.C. Specification Waveforms

8.1 A.C. Specification Table

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C; T_A = 0°C to +70°C

Symbol	Parameter	25 MHz		33 MHz		Units	Notes	Ref. Fig.
		Min	Max	Min	Max			
HOST INTERFACE SIGNALS								
HCLKCPU								
t1	Period (2x Mode)	20	28	15	21	ns	14	3
t1a	High Time	7		6.25		ns	14	3
t1b	High Time	4		4.5		ns	14	3
t1c	Low Time	7		6.25		ns	14	3
t1d	Low Time	5		4.5		ns	14	3
t1e	Rise/Fall Time		7		4	ns	1, 14	3
t1f	Period (1x Mode)	40	56	30	42	ns	15	3
t1g	High/Low Time			11		ns	15	3
t1h	Rise/Fall Time		4		3	ns	1, 15	3
t1i	High Time	17				ns	15, 17	3
t1j	Low Time	17.5				ns	15, 17	3
HKEN#								
t2	Setup to HCLKCPU Rising	20		15		ns		5
t2a	Hold from HCLKCPU Rising	1 CLK1		1 CLK1		ns		5
HADS0#/AS#								
t3	HADS0# Setup to HCLKCPU Rising	17		12		ns		6
t3a	HADS0# Hold from HCLKCPU Rising	1		1		ns		6
t3b	AS# Active Time	70		70		ns		7
t3c	AS# Inactive Time	15		15		ns		7
t3d	AS# Setup to HCLKCPU Rising	20		20		ns	2	7
t3e	AS# Hold from HCLKCPU Rising	10		10		ns	2	7
HADS1#								
t4	Setup to HCLKCPU Rising	17		10.5		ns		8
t4a	Hold from HCLKCPU Rising	2		2		ns		8
HBE[3:0]#								
t5	Setup to HCLKCPU Rising	12		10		ns		9
t5a	Hold from HCLKCPU Rising	1 CLK1		1 CLK1		ns		9
t5b	Propagation Delay from BE[3:0]#, or SA[1:0],SBHE#	2	18	2	18	ns		10
t5c	Setup to AS# Active	5		5		ns	1	11
t5d	Hold from ARDY Rising	0		0		ns		11
t5f	HBE[1:0]# Setup to SPWROK Rising	100		100		ns		13
t5g	HBE[1:0]# Hold from SPWROK Rising	0		0		ns		13
t5i	Float from HCLKCPU Rising		20		20	ns	1	14
t5j	Driven from HHLDA Rising	15		15		ns		14

8.1 A.C. Specification Table

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C; T_A = 0°C to +70°C (Continued)

Symbol	Parameter	25 MHz		33 MHz		Units	Notes	Ref. Fig.
		Min	Max	Min	Max			
HNA#/SBMODE#								
t6	HNA# Falling Valid Delay from HCLKCPU Rising	3	20	3	16	ns		15
t6a	HNA# Float Delay from HCLKCPU Rising		20		20	ns	1	15
t6b	HNA# Rising Valid Delay from HCLKCPU Rising		20		19	ns		15
t6c	SBMODE# Setup to SPWROK Rising	100		100		ns		16
t6d	SBMODE# Hold from SPWROK Rising	0		0		ns		16
HD/C#, HM/IO#, HW/R#								
t7	Setup to HCLKCPU Rising	10		6		ns		17, 18
t7a	Hold from HCLKCPU Rising	4		2		ns		17, 18
t7b	Setup to AS# Active	5		5		ns		19
t7c	Hold from ARDY Rising	0		0		ns		19
HD/C#, HM/IO#								
t8a	Float Delay from HCLKCPU Rising		20		20	ns	1, 3	21
t8b	Driven from HHLDA Rising	15		15		ns	3	21
HW/R#								
t9	Propagation Delay from W-R		30		30	ns		22
t9a	Propagation Delay from IOWC#, MWTC#		40		40	ns		23
t9b	Setup to BCLK Rising	20		20		ns		24
t9c	Float Delay from EXMASTER#, EMSTR16# and REFRESH#		25		25	ns	1, 3	25
t9d	Driven from EXMASTER#, EMSTR16# or REFRESH#	15		15		ns	3	25
HLOCMEM#, HLOCIO#								
t10	Setup to HCLKCPU Rising	15		12		ns		26
t10a	Hold from HCLKCPU Rising	2		2		ns		26
t10b	Setup to BCLK Rising	40		40		ns		27
t10c	Hold from BCLK Rising	½ BCLK		½ BCLK		ns		27
t10d	Setup to AS# Falling	−35		−30		ns		28
t10e	Hold from ARDY Rising	0		0		ns		28
HSTRETCH#								
t11	Setup to HCLKCPU Rising	20		15		ns	4	29
t11a	Hold from HCLKCPU Rising	1		1		ns	4	29

8.1 A.C. Specification Table

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C; T_A = 0°C to +70°C (Continued)

Symbol	Parameter	25 MHz		33 MHz		Units	Notes	Ref. Fig.
		Min	Max	Min	Max			
HRDYI#								
t12	HRDYI# Setup to HCLKCPU Rising	20		14.5		ns		30
t12a	HRDYI# Hold from HCLKCPU Rising	2		2		ns		30
HERDYO#/ARDY, HRDYO#/SDVLD								
t13	HRDYO# Valid Delay from HCLKCPU Rising	2	21	2	21	ns		33
t13a	HRDYO# Float Delay from HCLKCPU Rising		20		20	ns	1	33
t13b	SDVLD Pulse Width	15		15		ns	1	34
t13c	SDVLD Rising Valid Delay from BCLK Rising	15		15		ns		34
t13d	ARDY Falling from AS# Falling		230		180	ns		35, 16
t13e	ARDY Low Time	50		50		ns		35
t13f	HERDYO# Valid Delay from HCLKCPU Rising	2	24	2	21	ns		33
HHOLD								
t14	Valid Delay from HCLKCPU Rising	2	22	2	17	ns		36
HHLDA								
t15	Setup to HCLKCPU Rising	12		10		ns		37
HLOCK#								
t16	Setup to HCLKCPU Rising	10		7		ns		38, 39, 40
t16a	Hold from HCLKCPU Rising	2		2		ns		38, 39, 40
t16b	Setup to AS# Falling	−30		−30		ns		41
HSSTRB#								
t17	Valid Delay from HCLKCPU Rising	4	23	4	23	ns		42, 43, 44
QHSSTRB#								
t17a	Valid Delay from HCLKCPU Rising	4	23	4	23	ns		43, 44
HGT16M#								
t18	Setup to BCLK Rising	60		60		ns		45
t18a	Hold from BCLK Rising	60		60		ns		45
EISA BUS INTERFACE SIGNALS								
BE[3:0]#								
t19	Valid Delay from BCLK Falling	1	75	1	75	ns		46, 47, 48
t19a	Valid Delay from BCLK Rising	1	25	1	25	ns		48
t19b	Setup to BCLK Rising	80		80		ns		49
t19c	Hold from BCLK Rising	½ BCLK		½ BCLK				49
t19d	Propagation Delay from SA[1:0], SBHE#		60		60	ns		50
t19e	Setup to BCLK Falling (Burst)	30		30		ns		51
t19f	Hold from BCLK Falling (Burst)	2		2		ns		51
t19g	Falling Edge Propagation Delay from HKEN#		50		40	ns	i486 Only, 5	46
t19h	Propagation Delay from HBE#		40		30	ns		46

8.1 A.C. Specification Table

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C; T_A = 0°C to +70°C (Continued)

Symbol	Parameter	25 MHz		33 MHz		Units	Notes	Ref. Fig.
		Min	Max	Min	Max			
EISA BUS INTERFACE SIGNALS (Continued)								
M-IO								
t20	Propagation Delay from IORC#, IOWC#		40		40	ns		52
t20a	Setup to BCLK Rising	80		80		ns		53
t20b	Hold from BCLK Rising	½ BCLK		½ BCLK				53
W-R								
t21	Propagation Delay from IOWC#, MWTC#		60		60	ns		54
t21a	Propagation Delay from HW/R#		50		50	ns		55
t21b	Valid Delay from BCLK Falling	1	50	1	50	ns		55
t21c	Setup to BCLK Falling	25		25		ns		56
t21d	Hold from BCLK Rising	½ BCLK		½ BCLK				56
START#								
t22	Valid Delay from BCLK Rising	1	30	1	30	ns		57, 58
t22a	Valid Delay from HCLKCPU Rising	1	32	1	32	ns		58
t22b	Pulse Width	$T_{per}-5$		$T_{per}-5$		ns	1	59
t22c	Setup to BCLK Falling	23		23		ns		60
t22d	Hold from BCLK Rising	0		0		ns		60
t22e	Falling Edge Delay from AS# Falling	100		80		ns		61
CMD#								
t23	Valid Delay from BCLK Rising/Falling	1	30	1	30	ns		62, 63
t23a	Prop Delay from IORC#, MRDC#	0	30	0	30	ns		64
t23b	Pulse Width (Standard)	$T_{per}-5$		$T_{per}-5$		ns	1	65
MSBURST#								
t24	Valid Delay from BCLK Falling	1	35	1	35	ns		67
t24a	Setup to BCLK Rising	12		12		ns		66
t24b	Hold from BCLK Rising	1 CLK1 + 5		1 CLK1 + 15		ns		66
SLBURST#								
t25	Setup to BCLK Rising	15		15		ns		66, 67
t25a	Hold from BCLK Rising	25		25		ns		66, 67
EX32#, EX16#								
t26	Valid Delay from BCLK Falling	3	32	3	32	ns		68
t26a	Float Delay from BCLK Falling	2	19	2	19	ns	1	68
t26b	EX32# Propagation Delay from HLOCMEM#/HLOCIO# Falling		26		26	ns		69
t26c	EX32# Float Delay from HLOCMEM#/HLOCIO# Rising		14		14	ns	1	69
t26d	Setup to BCLK Rising	25		25		ns		70
t26e	Hold from BCLK Rising	55		55		ns		70

8.1 A.C. Specification Table

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C; T_A = 0°C to +70°C (Continued)

Symbol	Parameter	25 MHz		33 MHz		Units	Notes	Ref. Fig.
		Min	Max	Min	Max			
EISA BUS INTERFACE SIGNALS (Continued)								
EXRDY								
t27	Valid Delay from BCLK Rising	1	32	1	32	ns		71
t27a	Setup to BCLK Falling	13		13		ns		72
t27b	Hold from BCLK Falling	0		0		ns		72
t27c	Float Delay from BCLK Falling	2	30	2	30	ns	1	71
LOCK#								
t28	Valid Delay from BCLK Rising	1	40	1	40	ns		73, 74, 75
BALE								
t29	BALE Rising Edge Valid Delay from BCLK Falling	1	20	1	20	ns		76
t29a	BALE Falling Edge Valid Delay from BCLK Rising	1	25	1	25	ns		76
t29b	BALE Rising from HCLKCPU Rising	1	30	1	30	ns		76
MASTER16#								
t30	Setup to BCLK Rising	17		17		ns		77
t30a	Hold from BCLK Rising	0		0		ns		77
BCLKOUT								
t31	Valid Delay from HCLKCPU Rising/Falling	1	15	1	15	ns		78
t31a	Low Time	55		55		ns		4
t31b	Rise, Fall Time		5		5	ns	1	4
t31c	High Time	56		56		ns		4
t31d	Valid Delay from HCLKCPU Rising/Falling (50 pF)		11.5		11.5	ns		78
BCLKIN								
t31e	Return Delay from HCLKCPU Rising/Falling		20		20	ns	18, 19	78
t31f	Low Time	55		55		ns	18	4
t31g	High Time	56		56		ns	18	4
t31h	Cycle Time	120		120		ns	18	4
IORC#, IOWC#, MRDC#, AND MWTC#								
t32	Valid Delay from BCLK Rising/Falling	2.0	30	2.0	30	ns	6	79
t32a	IOWC# Valid Delay from BCLK Rising/Falling	3.5	25	3.5	25	ns		79
SMRDC#, SMWTC#								
t33	Propagation Delay from MRDC#, MWTC#		25		25	ns		80, 81
t33a	Falling Edge Propagation Delay from GT1M# Rising		40		40	ns		81
t33b	Valid Delay from BCLK Rising/Falling	2	30	2	30	ns		82
M16#								
t34	Setup to BCLK Rising	18		18		ns		83
t34a	Hold from BCLK Falling	0		0		ns		83
IO16#								
t35	Setup to BCLK Falling	20		20		ns		84
t35a	Hold from BCLK Falling	20		20		ns		84
t35b	Propagation Delay from HLOCIO# Falling		70		70	ns		85
t35c	Float Delay from HLOCIO# Rising		70		70	ns		85

8.1 A.C. Specification Table

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C; T_A = 0°C to +70°C (Continued)

Symbol	Parameter	25 MHz		33 MHz		Units	Notes	Ref. Fig.
		Min	Max	Min	Max			
EISA BUS INTERFACE SIGNALS (Continued)								
CHRDY								
t36	Propagation Delay from MRDC#, MWTC#, IORC#, IOWC#		60		60	ns		86
t36a	Float Delay from BCLK Falling		15		15	ns	1	86
t36b	Input Pulse Width (When Low)	10		10		ns		87
t36c	Falling Edge Setup to BCLK Falling	7		7		ns		87
t36d	Rising Edge Setup to BCLK Rising	10		10		ns		87
NOWS#								
t37	Setup to BCLK Falling	10		10		ns		88, 89
t37a	Hold from BCLK Falling	20		20		ns		88, 89
SA[1:0], SBHE#								
t38	Propagation Delay from BE[3:0]#		40		40	ns	7	90, 91
t38a	Valid Delay from BCLK Falling		30		30	ns		92, 93
REFRESH#								
t39	Setup to BCLK Rising	18		18		ns		94, 95
t39a	Hold from BCLK Rising	3		3		ns		95
ISP INTERFACE SIGNALS								
ST[3:0]								
t42	ST0 Valid Delay from HCLKCPU Rising	1	23	1	23	ns		96
t42a	ST0 Prop Delay from START# Falling		25		25	ns		97
t42c	ST2 Prop Delay from HD/C#, HM/IO#, HW/R# Falling		40		40	ns		96
t42d	ST2 Valid Delay from BCLK Falling (Pipelined)	1	40	1	40	ns		96
EXMASTER#								
t43	Setup to BCLK Rising	15		15		ns		98
EMSTR16#								
t44	Setup to BCLK Rising	15		15		ns		99
DATA BUFFER CONTROL SIGNALS								
SDCPYEN01#, SDCPYEN02#, SDCPYEN03#, SDCPYEN13#								
t45	Valid Delay from BCLK Rising/Falling	4	21	4	21	ns	8, 9	100, 101, 102, 103
t45a	Propagation Delay from IO16# Falling		20		20	ns		104
t45b	Rising Edge Valid Delay from BCLK Rising/Falling	2	20	2	20	ns		102, 103, 105
t45c	Falling Edge Valid Delay from BCLK Falling	1	15	1	15	ns		105
t45d	Falling Edge Valid Delay from BCLK Rising		27		27	ns		106
t45e	SDCPYUP Setup to SDCPYEN01#	0		0		ns		106
t45f	Propagation Delay from MWTC#, IOWC#	2	20	2	20	ns		107, 108, 109
t45g	Propagation Delay from MRDC#, IORC#		35		35	ns		107, 108, 109
t45h	SDCPYEN01# Valid Delay from BCLK Rising/Falling	2	25	2	25	ns		109

8.1 A.C. Specification Table

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C; T_A = 0°C to +70°C (Continued)

Symbol	Parameter	25 MHz		33 MHz		Units	Notes	Ref. Fig.
		Min	Max	Min	Max			
DATA BUFFER CONTROL SIGNALS (Continued)								
SDCPYUP								
t46	Valid Delay from BCLK Rising/Falling	1	25	1	25	ns	8	110, 111
t46a	Propagation Delay from MWTC#, IOWC#	2	20	2	20	ns		112, 113
t46b	Propagation Delay from MRDC#		35		35	ns		114
t46c	Valid Delay from BCLK Rising/Falling	2	25	2	25	ns		113
SDHDLE[3:0]#								
t47	Valid Delay from BCLK Rising/Falling	1	25	1	25	ns		115, 116
t47a	Driven High before CMD#, MRDC#, IORC#, SMRDC# Driven High	2.0		2.0		ns	AS	116
t47b	Driven High before SDCPYEN[3:0]# Driven High	2		2		ns	AS	116
t47c	Propagation Delay from MWTC#, IOWC#		25		25	ns		117
SDOE[2:0]#								
t48	Valid Delay from BCLK Rising/Falling	1	15	1	15	ns		118, 119
t48a	Valid Delay from BCLK Rising	10	40	10	40	ns	5, 10	120
t48b	Valid Delay from BCLK Falling	1	25	1	25	ns	11	120, 121
t48c	Falling Edge Prop Delay from IORC#, MRDC#		54		54	ns		122
t48d	Valid Delay from BCLK Rising/Falling	1	31	1	31	ns		123
HDSDLE1#								
t49	Valid Delay from BCLK Rising/Falling	1	15	1	15	ns		124, 125
t49a	Valid Delay from BCLK Falling, HCLKCPU Rising	1	25	1	25	ns		126
t49b	Falling Edge Prop Delay from MRDC#/IORC# Falling		30		30	ns		127
t49c	Driven High before HDOE# Drive High	0		0		ns		124
HDOE[1:0]#								
t50	Valid Delay from BCLK Rising/Falling, HCLKCPU Rising	4	25	4	25	ns		128, 129, 130
t50a	Propagation Delay from MWTC#/IOWC#		25		25	ns		131
ADDRESS BUFFER CONTROL SIGNALS								
HALAOE#								
t51	Prop Delay from EXMASTER#, EMSTR16#, or REFRESH#	3	30	3	30	ns		132
t51a	Prop Delay from HHLDA Rising	6	50	6	50	ns		132
t51b	Prop Delay from HHOLD Falling	1	30	1	30	ns		132
LASAOE#								
t52	Propagation Delay from EMSTR16#, REFRESH#		30		30	ns		133
LAHAOE#								
t53	Propagation Delay from EXMASTER#, EMSTR16#		35		35	ns		134
t53a	Propagation Delay from HHLDA Rising/Falling	1	50	1	50	ns		134
t53b	Valid Delay from BCLK Rising	1	40	1	40	ns	12	134
LALE#								
t54	Valid Delay from BCLK Rising/Falling, or HCLKCPU Rising	1	30	1	30	ns		135, 136, 137

8.1 A.C. Specification Table

Functional Operating Range: V_{CC} = 5V ±5%; T_{CASE} = 0°C to +85°C; T_A = 0°C to +70°C (Continued)

Symbol	Parameter	25 MHz		33 MHz		Units	Notes	Ref. Fig.
		Min	Max	Min	Max			
MISCELLANEOUS SIGNALS (Continued)								
SALAOE#								
t55	Propagation Delay from EMSTR16#, REFRESH#		35		35	ns		138
SALE#								
t56	Valid Delay from BCLK Rising/Falling	1	14	1	14	ns	13	139
t56a	Valid Delay from BCLK Rising	1	38	1	38	ns		140
MISCELLANEOUS SIGNALS								
SPWROK								
t57	Setup to HCLKCPU Rising	6		6		ns		141
t57a	Hold from HCLKCPU Rising	0		0		ns		141
RST								
t58	Valid Delay from HCLKCPU Rising	1	21	1	21	ns		142
RSTCPU, RST385								
t59	Valid Delay from HCLKCPU Rising/Falling	2	21	2	21	ns		142, 143, 144
CLKKB								
t60	Period	90	120	90	120	ns		4
t60a	High, Low Time	25	80	25	80	ns		4
t60b	Valid Delay from HCLKCPU Rising/Falling	1	40	1	40	ns		145
t60c	Rise, Fall Time		10		10	ns	1	4
LIOWAIT#								
t61	Setup to BCLK Rising	35		35		ns		146
t61a	Hold from BCLK Rising	0		0		ns		146
AENLE#								
t62	Valid Delay from BCLK Falling	1	30	1	30	ns		147
t62a	Valid Delay from HCLKCPU Rising	1	45	1	45	ns		147
PWEN#								
t63	Setup to HCLKCPU Rising	14		14		ns		148
t63a	Hold from HCLKCPU Rising	2		2		ns		148
t63b	Setup to AS# Falling	−35		−30		ns		149
t63c	Hold from ARDY Rising	0		0		ns		149

NOTES:
AS = Assembly cycles.
1. Sampled, not 100% tested.
2. Asynchronous input. These specifications must be met if an exact cycle length determination is required.
3. HM/IO# and HW/R# are outputs only when AMODE is strapped low.
4. HSTRETCH# can not be held low for more than 400 ns.
5. Active edge only.
6. This spec applies to MRDC#, MWTC#, and IORC# only.
7. SBHE# is not active for ISA master REFRESH cycles.
8. Assumes tracking between the SDCPYEN#, SDCPYUP outputs and the MWTC#, SMWTC# outputs. (Specifically, a 20 ns output delay for the copy enables assumes a minimum delay on MWTC#, SMWTC# of 7 ns.)
9. Read cycles are not specified because system timings guarantee adequate timing margins for the SDCPYENx# signal paths.

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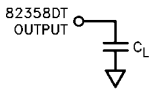
10. This spec applies to write cycles requiring EISA master back-off (i.e., the first cycle of a disassembly).
11. This spec is for a write disassembly, except the first cycle of EISA or DMA bus masters.
12. This applies to the BCLK rising edge after REFRESH# goes inactive during ISA master refresh cycles.
13. This spec only applies to cases where BCLK is not stretched, since BCLK stretched cases are not critical.
14. 386 only.
15. i486 only.
16. Typical values for t13d are:

Back to Back Cycles		Single Cycles	
25 MHz	**33 MHz**	**25 MHz**	**33 MHz**
170 ns	140 ns	130 ns	110 ns

17. The 82358DT will function correctly with a HCLKCPU high and low time of 15 ns. However, A.C. specs t1i and t1j are required to guarantee a BCLK high time of 56 ns and a BCLK low time of 55 ns.
18. BCLKIN is an input. It is the software designer's responsibility to ensure that all BCLKIN specs are met with the system's BCLK distribution structure. The waveform on BCLKIN must replicate BCLKOUT (i.e., direct connect of BCLKOUT to BCLKIN or through a non-inverting buffer) though possibly delayed as specified.
19. The return delay must satisfy t31e when measured at the V__ih and V__il levels specified for the BCLKIN input.

8.2 A.C. Test Loads



290380-X0

C_L = Minimum Valid Delay Spec Capacitive Load = 50 pF
C_L = Maximum Specification Capacitive Load = 50 pF: HHOLD, SDCPYEN01#, SDCPYEN02#, SDCPYEN03#, SDCPYEN13#, SDHDLE[3:0]#, SDOE[2:0]#, HDSDLE1#, HDOE[1:0]#, HALAOE#, HALE#, LASAOE#, LAHAOE#, LALE#, SALAOE#, SALE#, HERDYO#/ARDY, DRDY, ST[3:0], RST, RSTCPU, RST385, AENLE#, HNA#/SBMODE.

80 pF: SDCPYUP, CLKKB
120 pF: HM/IO#, HW/R#, HD/C#, HRDYO#/SDVLD, HBE[3:0]#, HSSTRB#, QHSSTRB#.
240 pF: BE[3:0]#, M-IO#, W-R#, START#, CMD#, MSBURST#, SLBURST#, EX32#, EX16#, EXRDY, LOCK#, BALE, BCLKOUT, IORC#, IOWC#, MRDC#, MWTC#, SMRDC#, SMWTC#, IO16#, M16#, CHRDY, SA[1:0], SBHE#.

C_L includes all parasitic capacitances.

Figure 8-2. A.C. Test Loads

8.3 A.C. Timing Diagrams

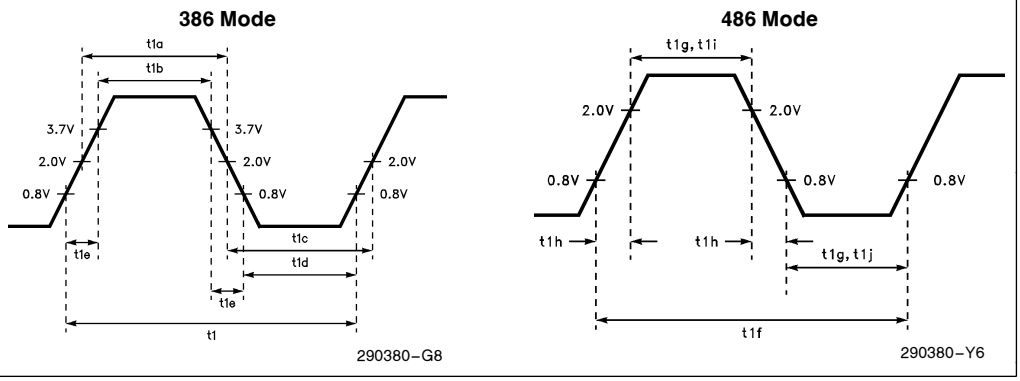


Figure 8-3. HCLKCPU Timing—t1–t1j

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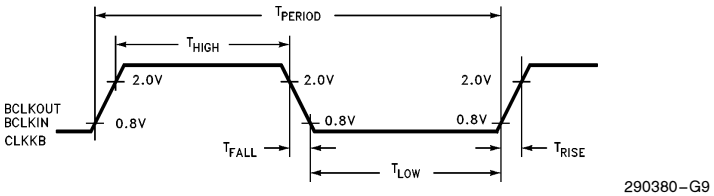


T_{HIGH} = t31c, t60a, t31g
T_{LOW} = t31a, t60a, t31f
T_{RISE} = t31b, t60c
T_{FALL} = t31b, t60c
T_{PERIOD} = t60, t31h

Figure 8-4. BCLK and CLKKB Timing—t31a, t31b, t60, t60a, t60c, t60d

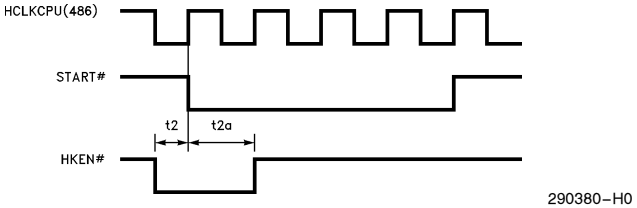


Figure 8-5. i486™ Host Memory Read Cycle to the EISA/ISA Bus—t2, t2a

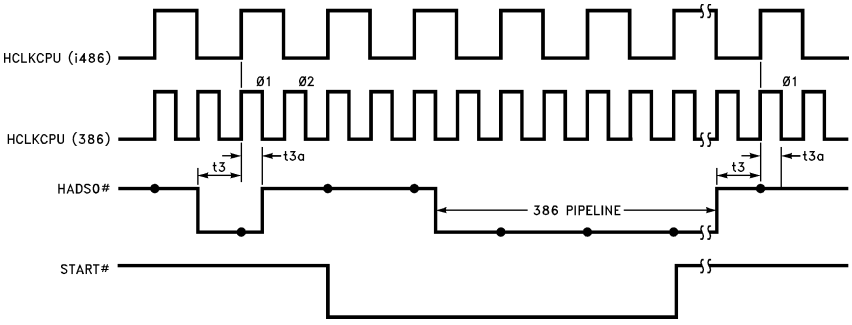


Figure 8-6. Host Master Cycle to the EISA/ISA Bus (82350 System)—t3, t3a

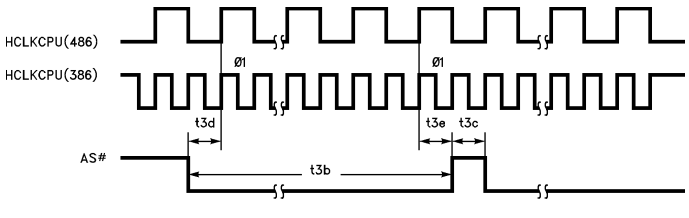


Figure 8-7. Host Master Cycle to the EISA/ISA Bus (82350DT System)—t3b through t3e

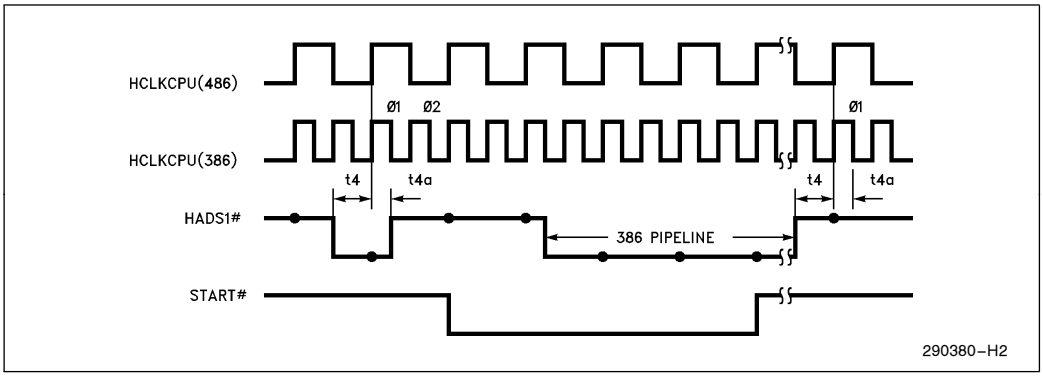


Figure 8-8. Host Master Cycle to the EISA/ISA Bus (82350 System)—t4, t4a

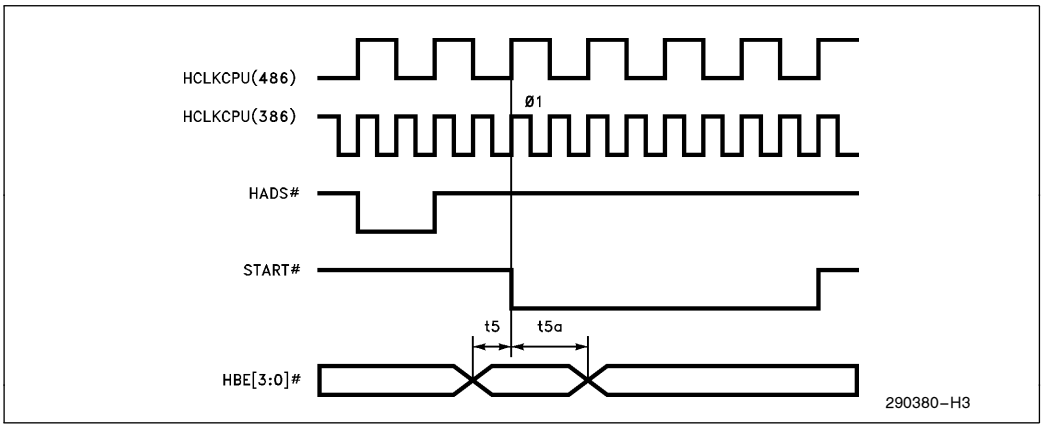


Figure 8-9. Host Master Cycle to the EISA/ISA Bus (82350 System)—t5, t5a

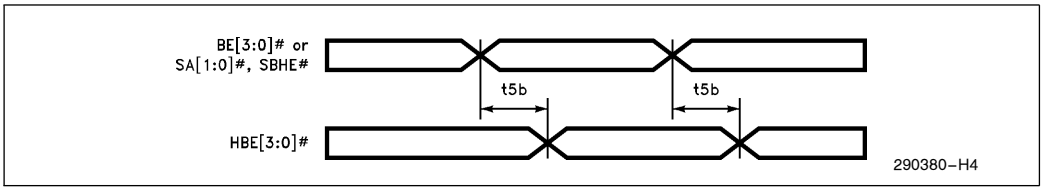


Figure 8-10. EISA, ISA, DMA, or REFRESH Master Cycle to the Host Bus—t5b

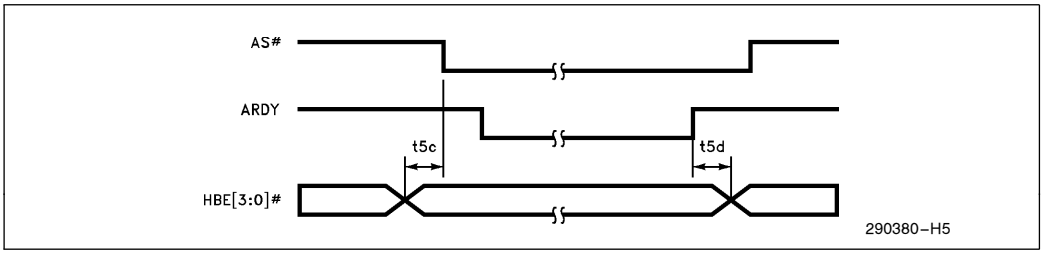


Figure 8-11. Host Master Cycle to the EISA/ISA Bus (82350DT System)—t5c, t5d

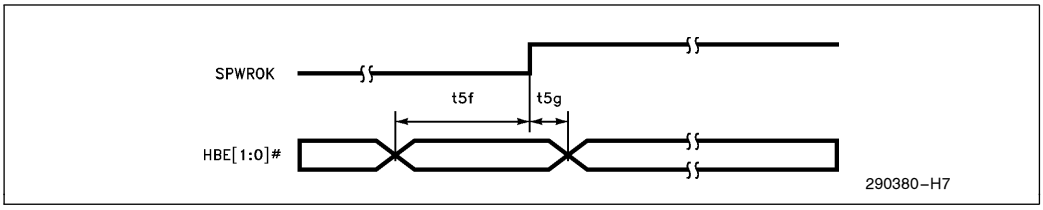


Figure 8-12. HBE[1:0]# Setup and Hold During Power-Up—t5f, t5g

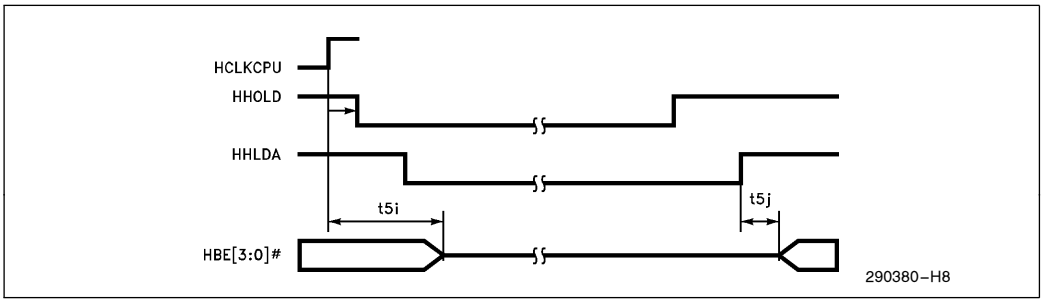


Figure 8-13. HBE[3:0]# Float and Drive Timing—t5i, t5j

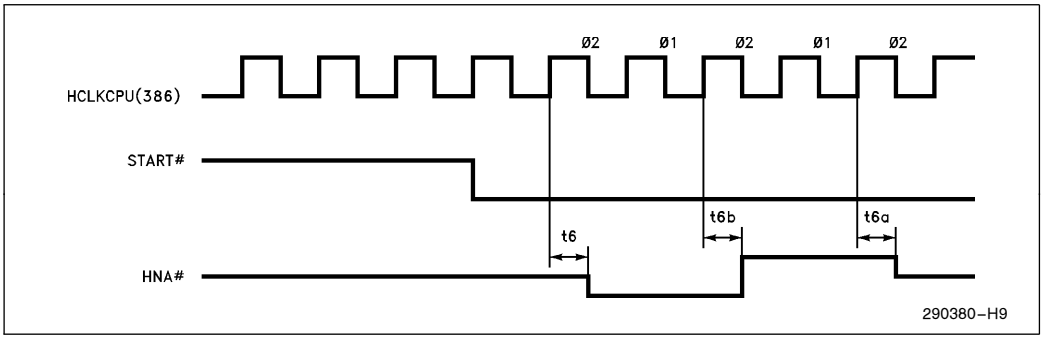


Figure 8-14. Host Master Cycle to the EISA/ISA Bus—t6, t6a, t6b

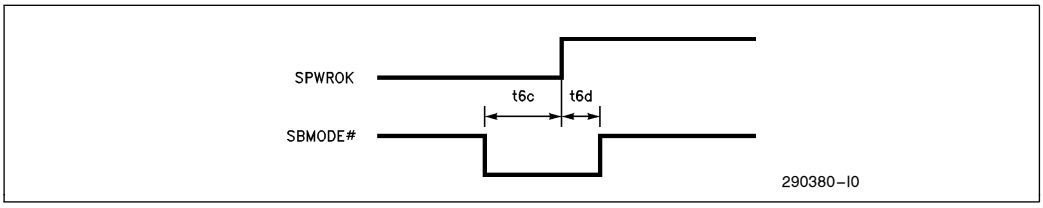


Figure 8-15. SBMODE# Setup and Hold During Power-Up—t6c, t6d

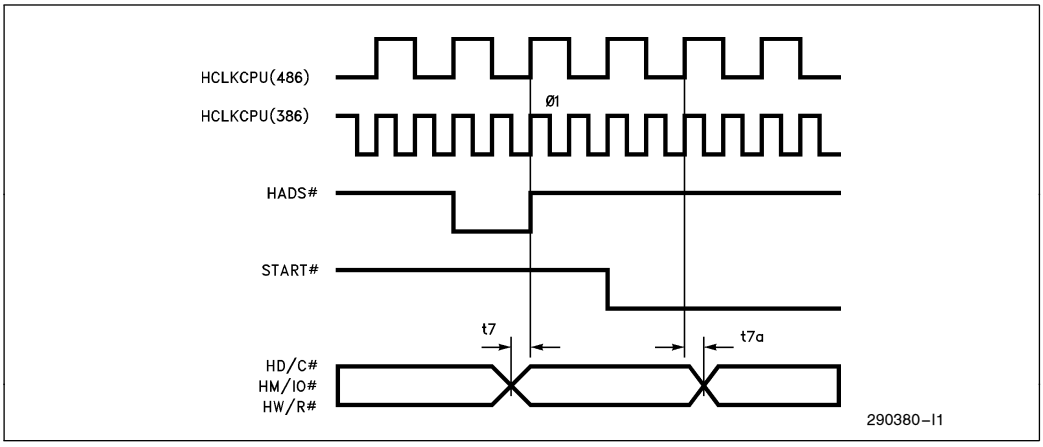


Figure 8-16. Host Master Cycle to the EISA/ISA Bus (82350 System)—t7, t7a

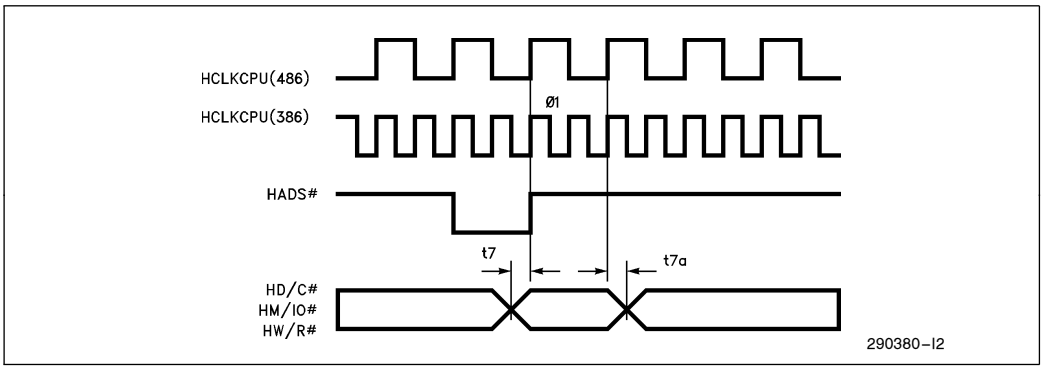


Figure 8-17. Host Master Cycle to Host Slave (82350 System)—t7, t7a

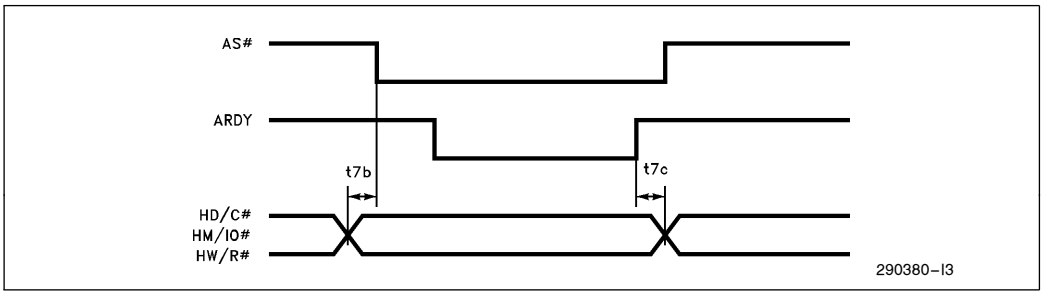


Figure 8-18. Host Master Cycle to the EISA/ISA Bus (82350DT System)—t7b, t7c

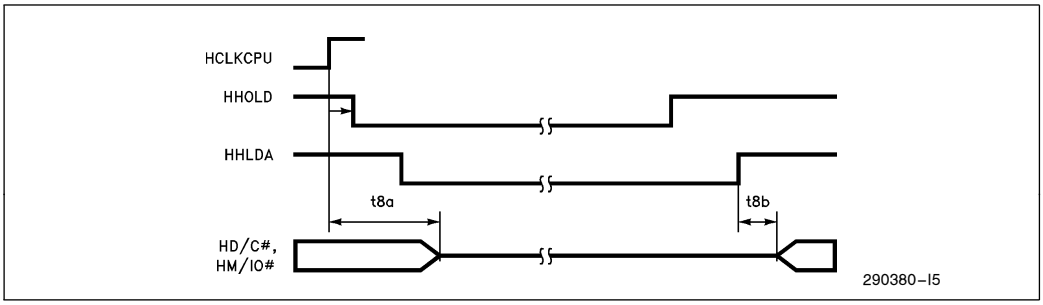


Figure 8-19. HD/C#, HM/IO# Float and Drive Timing—t8a, t8b

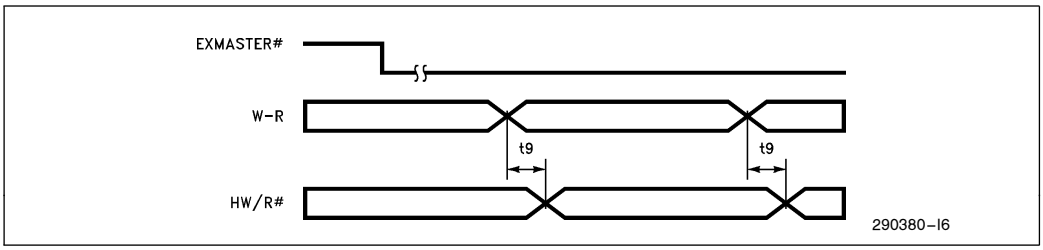


Figure 8-20. EISA Master Cycle (82350, 82350DT/Buffered Systems)—t9

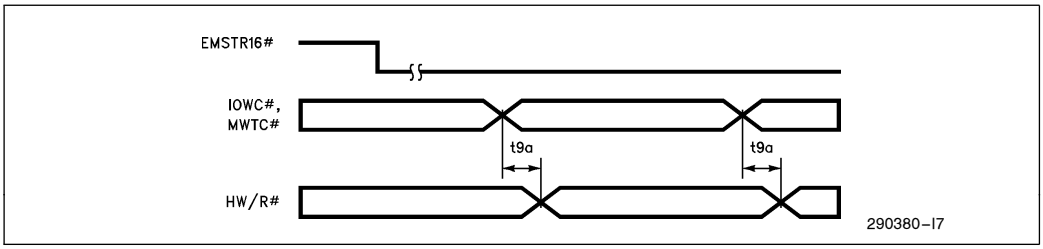


Figure 8-21. ISA Master Cycle (82350, 82350DT/Buffered Systems)—t9a

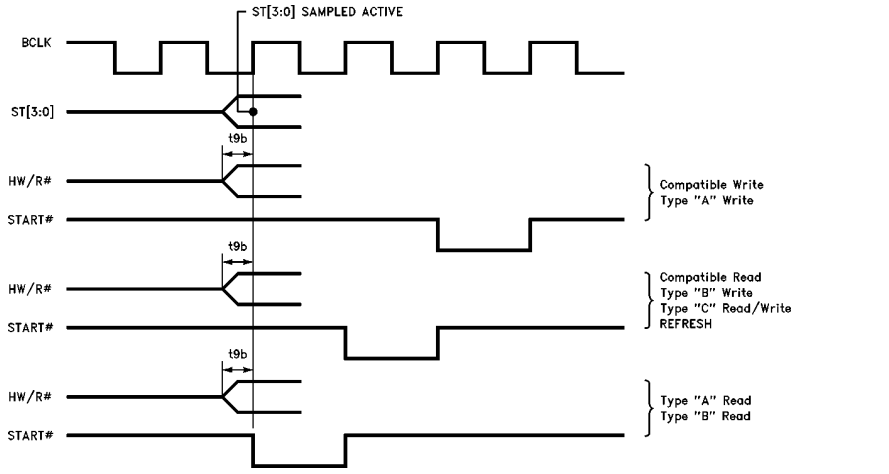
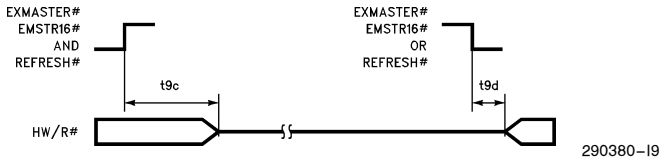
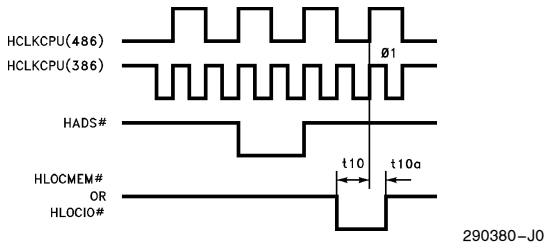


Figure 8-22. DMA or REFRESH Master Cycle—t9b



EXMASTER#, EMSTR16#, and REFRESH# are "ANDed" together to float HW/R#. HW/R# floats from the rising edge of the last signal to transition high from this signal group. HW/R# is driven from the falling edge of the first signal to transition low from this signal group.

Figure 8-23. HW/R# Float and Drive Timing (82350, 82350DT/Buffered Systems)—t9c, t9d



In the case of back-to-back cycles (except back-to-back cycles where the first cycle is a posted write), HLOCMEM# and HLOCIO# are sampled on the rising edge of HCLKCPU, at the rising edge of the CMD# signal from the first cycle. If the first cycle is an assembly or disassembly cycle, HLOCMEM# and HLOCIO# are sampled at the end of the last CMD# of the assembly or disassembly process. In the case of back-to-back cycles where the first cycle is a posted write, HLOCMEM# and HLOCIO# for the second cycle are sampled on the same rising edge of HCLKCPU that HRYDI# from the first cycle is sampled active.

Figure 8-24. Host Master Cycle to the EISA/ISA Bus (82350 System)—t10, t10a

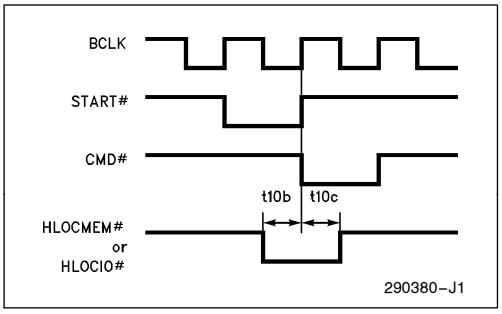


Figure 8-25. EISA or DMA Master Cycle—t10b, t10c

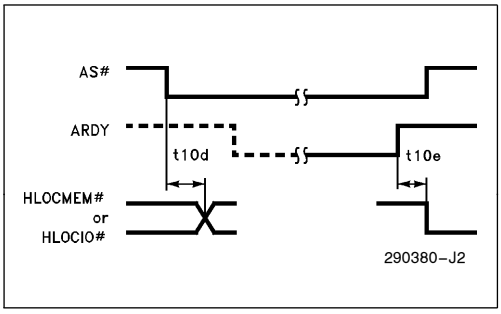


Figure 8-26. Host Master Cycle (82350DT System)—t10d, t10e

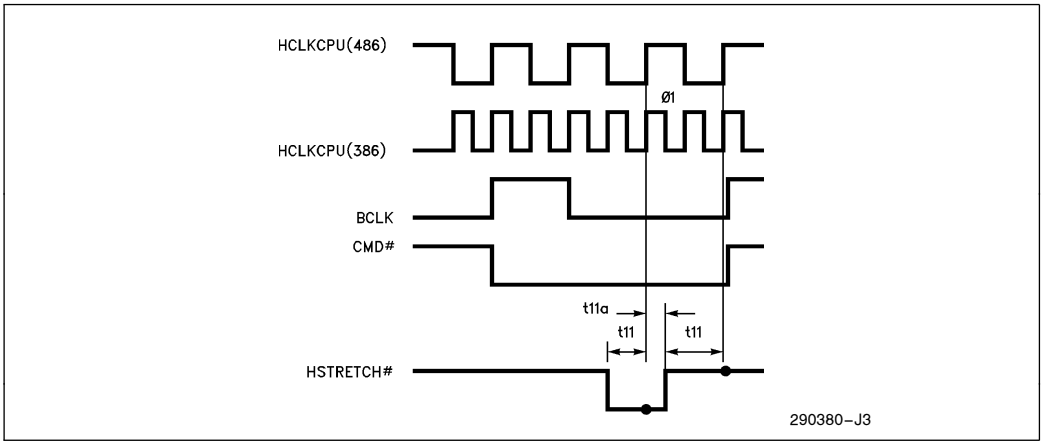


Figure 8-27. EISA, ISA, or DMA Master Cycle to the Host Bus—t11, t11a

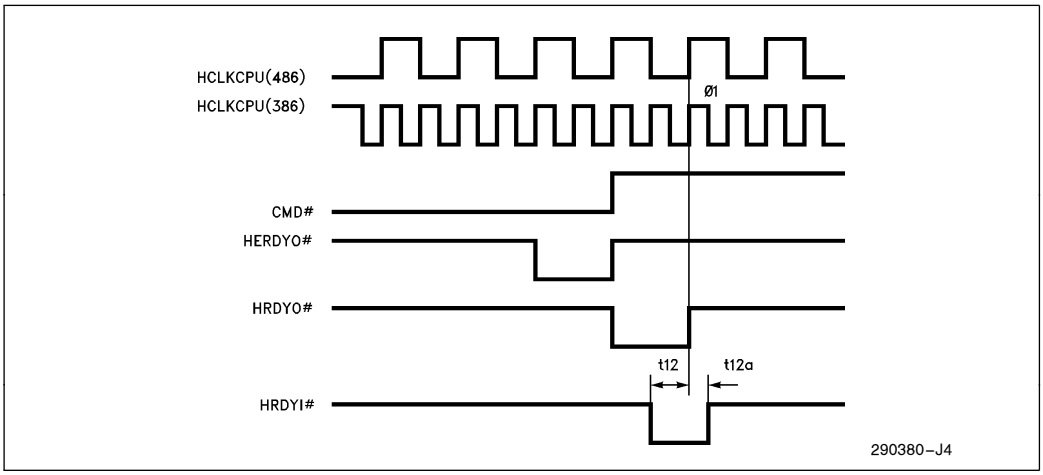


Figure 8-28. Host Master Cycle (82350 System)—t12, t12a

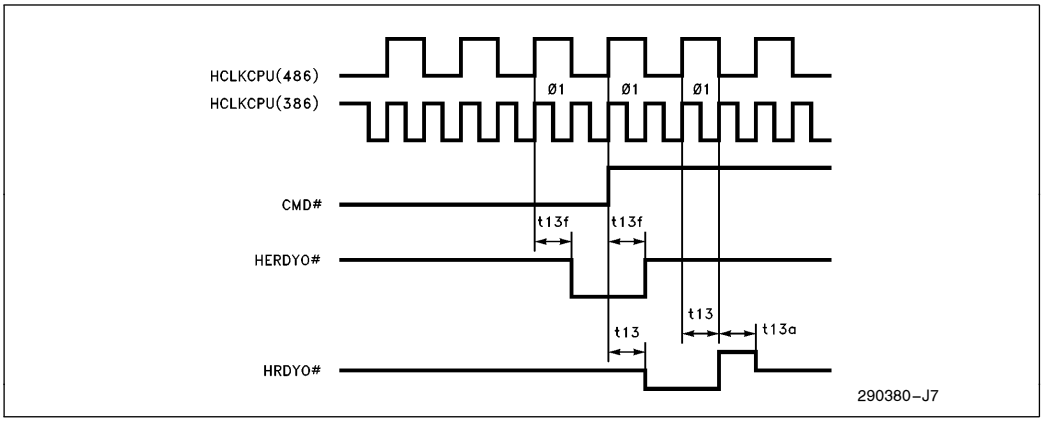
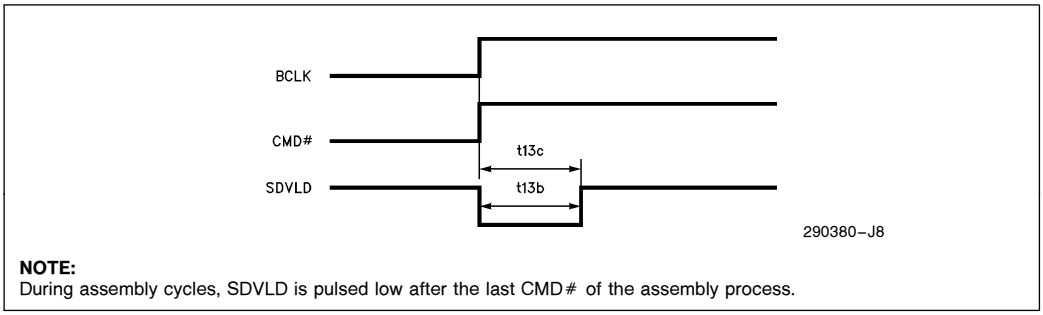


Figure 8-29. Host Master Cycle to the EISA/ISA Bus (82350 System)—t13, t13a



NOTE:
During assembly cycles, SDVLD is pulsed low after the last CMD# of the assembly process.

Figure 8-30. Host Master Read Cycle from the EISA/ISA Bus (82350DT System)—t13b, 13c

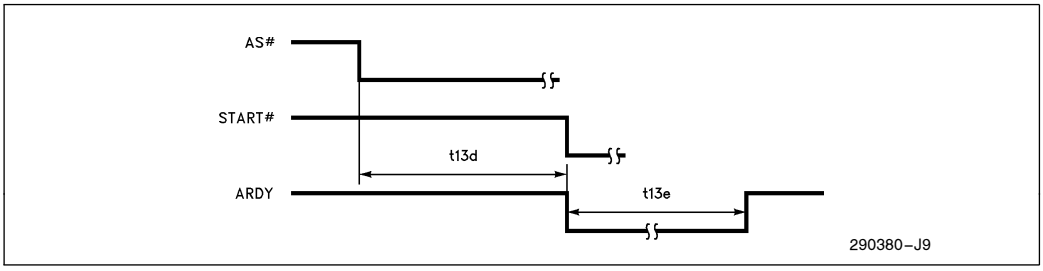


Figure 8-31. Host Master Cycle (82350DT System)—t13d, t13e

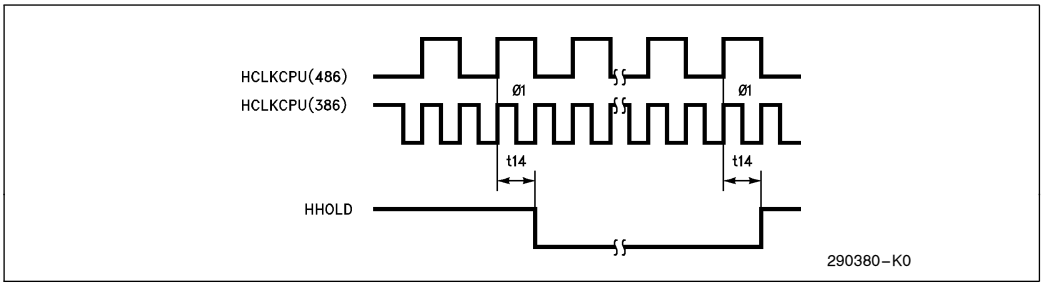


Figure 8-32. HHOLD Valid Delay (All Cycles)—t14

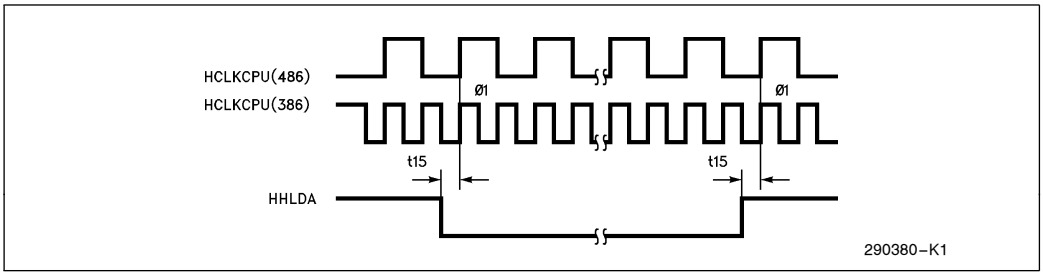


Figure 8-33. HHLDA Setup Timing (All Cycles)—t15

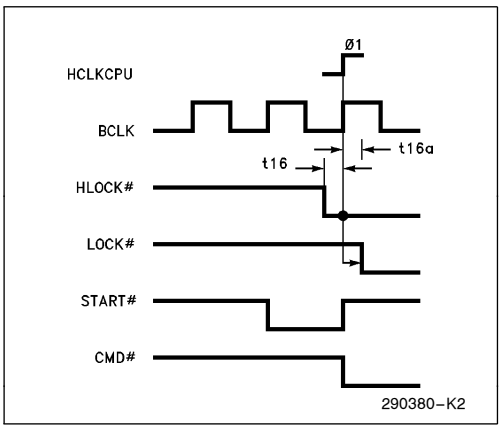


Figure 8-34. First Cycle of a LOCK—t16, t16a

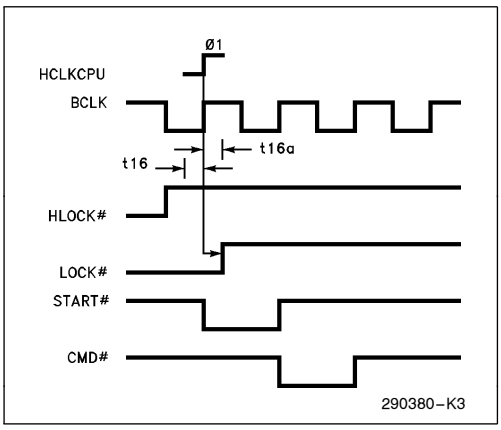


Figure 8-35. End of LOCK Where HLOCK# Is Sampled Inactive on the Following Cycles START#—t16, t16a

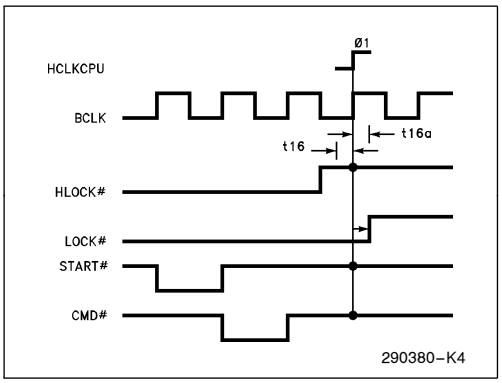


Figure 8-36. End of LOCK at BCLK Rising Where HLOCK#, START#, and CMD# Are Sampled Inactive on the Rising Edge of HCLKCPU—t16, t16a

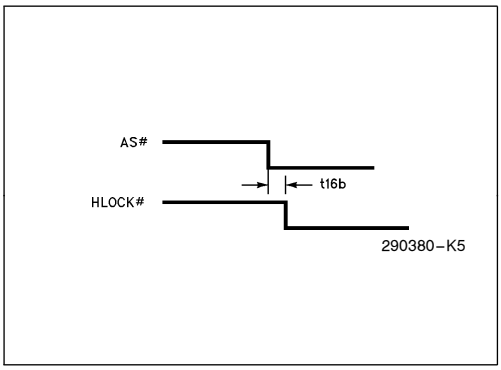


Figure 8-37. First Cycle of a LOCK (82350DT System)—t16b

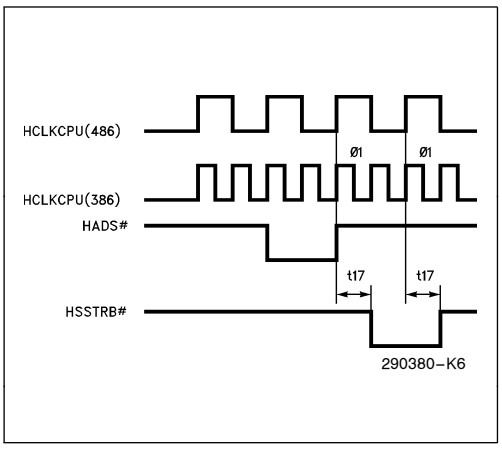


Figure 8-38. Host Master Memory Write Cycle—t17

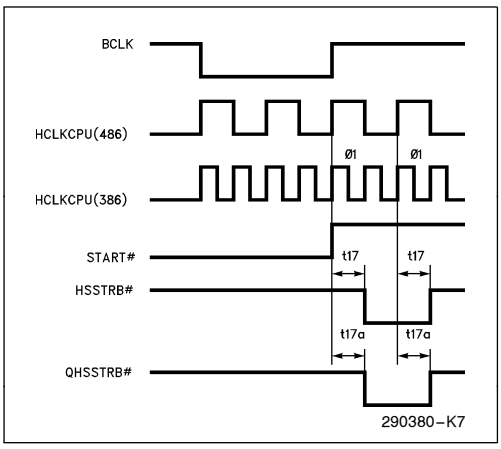


Figure 8-39. EISA, ISA, DMA, or REFRESH Master Memory Write Cycle (Except ISA Master to ISA Memory Slave)—t17, t17a

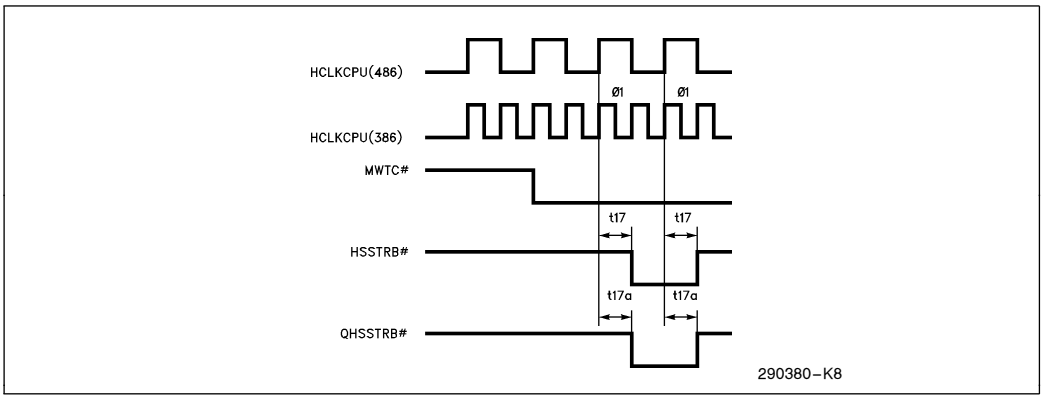


Figure 8-40. ISA Master Memory Write Cycle to ISA Slave—t17, t17a

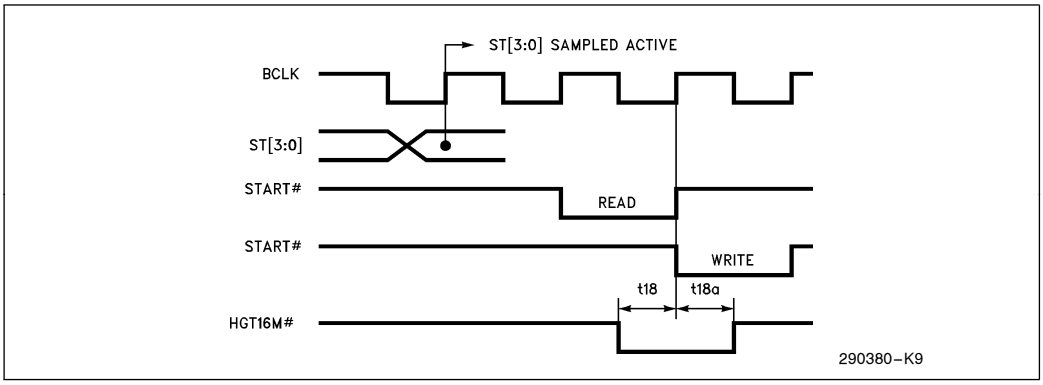


Figure 8-41. DMA Compatible Cycle—t18, t18a

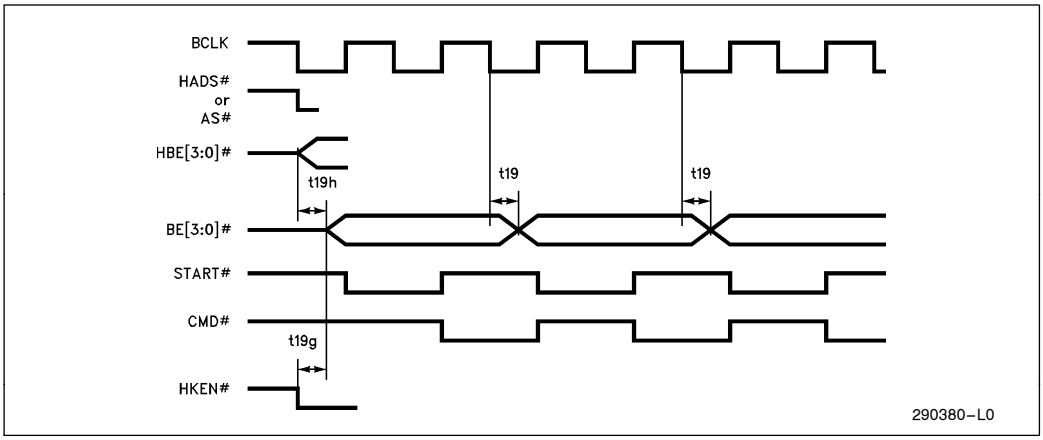


Figure 8-42. Host Master Cycle to the EISA/ISA Bus—t19, t19g, t19h

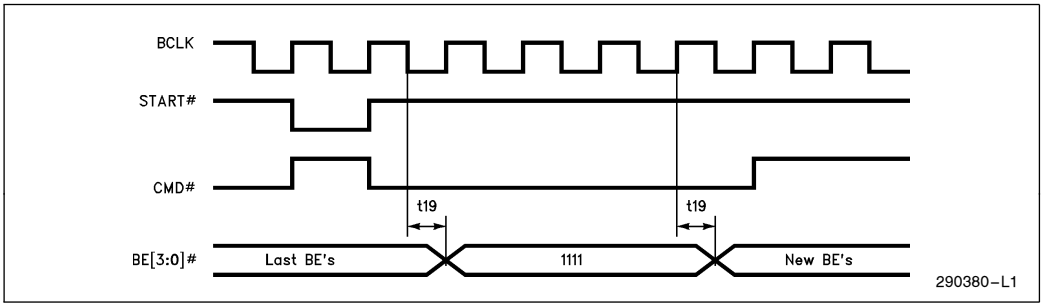


Figure 8-43. Host Master Cycle to an ISA Slave. Last Cycle of an Assembly or Disassembly Cycle (Except to a 16-Bit ISA with NOWS# Asserted)—t19

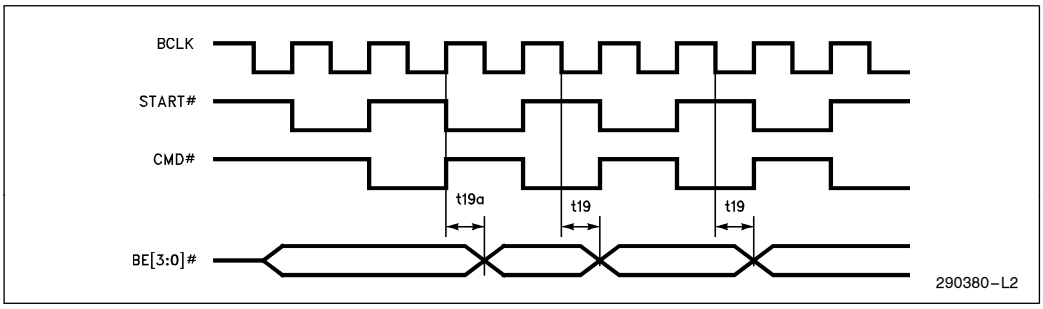


Figure 8-44. DMA Assembly or Disassembly Cycle—t19, t19a

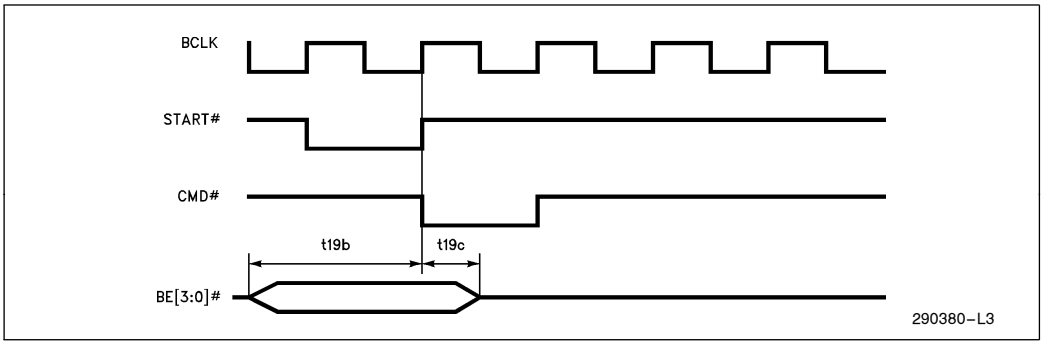


Figure 8-45. EISA or DMA Master Cycle—t19b, t19c

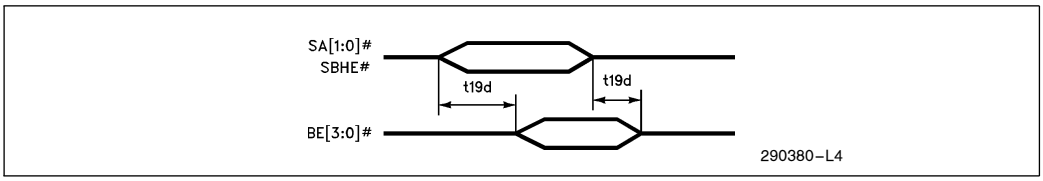


Figure 8-46. ISA Master Cycle—t19d

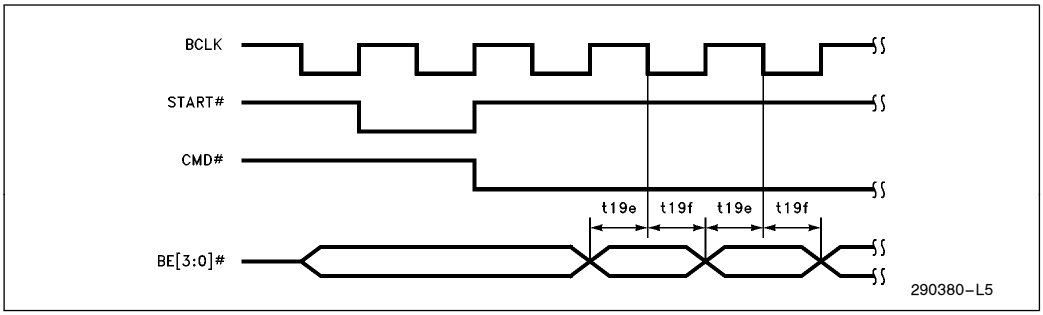


Figure 8-47. EISA or DMA Master Burst Cycle—t19e, t19f

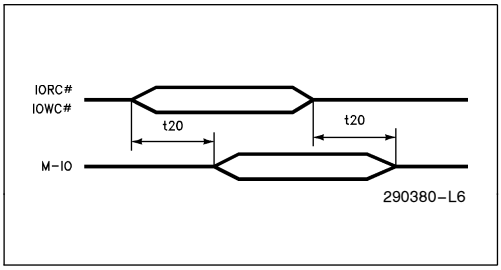


Figure 8-48. ISA Master Cycle—t20

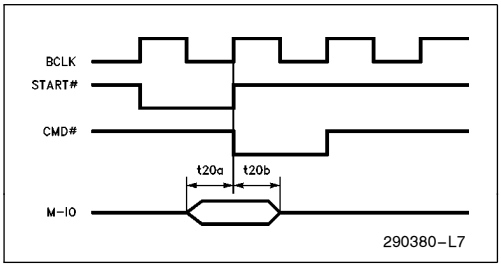


Figure 8-49. EISA Master Cycle—t20a, t20b

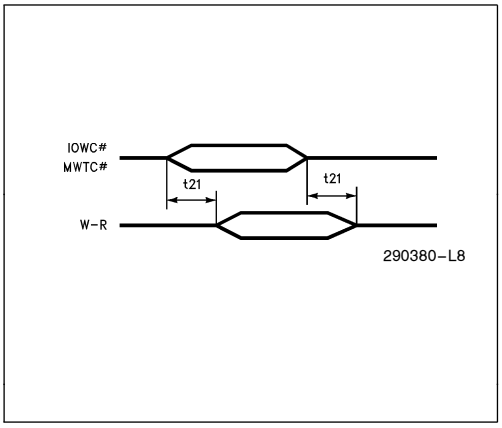
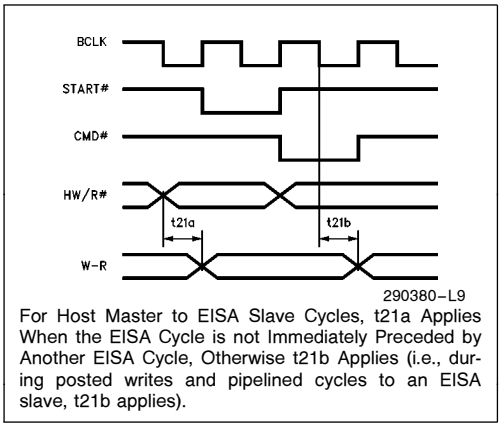


Figure 8-50. ISA Master Cycle—t21



For Host Master to EISA Slave Cycles, t21a Applies When the EISA Cycle is not Immediately Preceded by Another EISA Cycle, Otherwise t21b Applies (i.e., during posted writes and pipelined cycles to an EISA slave, t21b applies).

Figure 8-51. HOST, DMA, or REFRESH Master Cycle (82350, 82350DT/Buffered Systems)—t21a, t21b

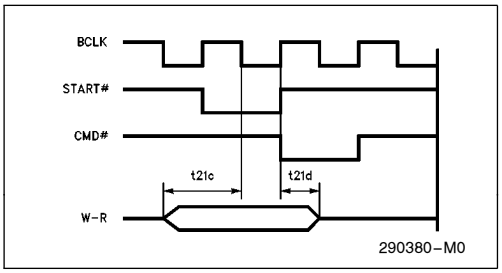


Figure 8-52. EISA Master Cycle—t21c, t21d

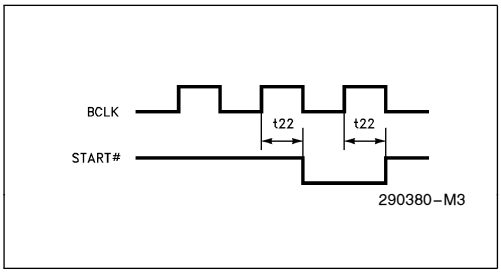


Figure 8-53. HOST, EISA Master Assembly/Disassembly, ISA, DMA, or REFRESH Master Cycle—t22

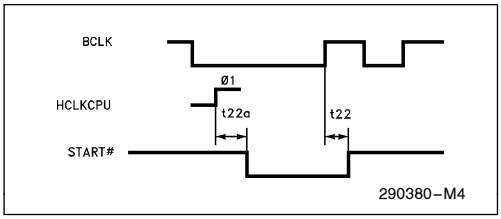


Figure 8-54. HOST or ISA Master Cycle when BCLK is Stretched—t22, t22a

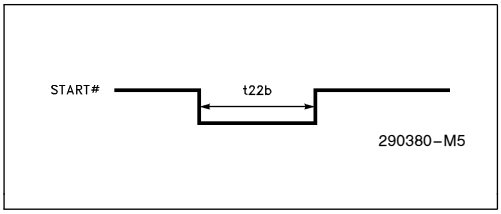


Figure 8-55. START# Pulse Width (All)—t22b

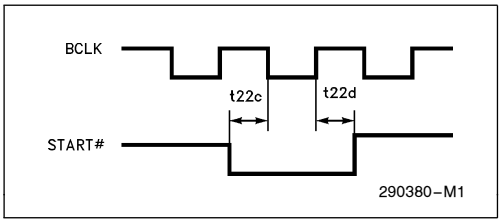


Figure 8-56. EISA Master Cycle—t22c, t22d

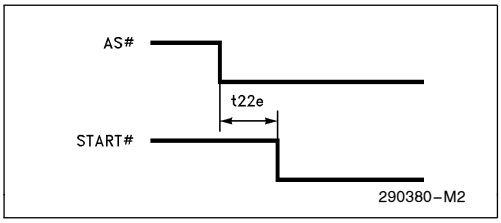


Figure 8-57. Host Master Cycle (82350DT System)—t22e

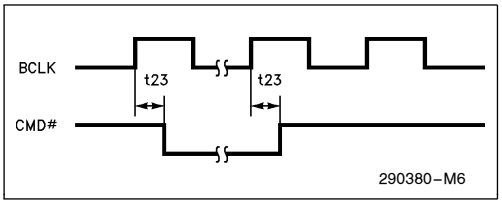


Figure 8-58. CMD# Valid Delay (General Case)—t23

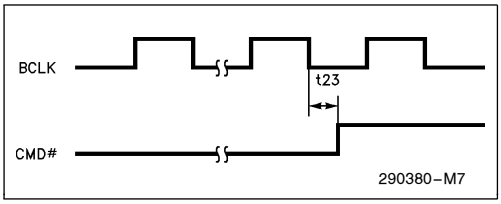


Figure 8-59. CMD# Special Case (Refer to Table 3-2)—t23

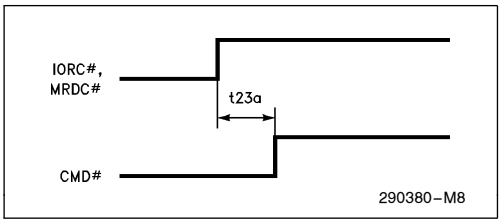


Figure 8-60. ISA Read Cycle—t23a

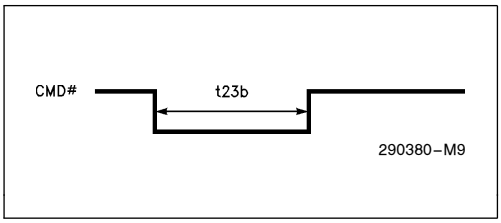


Figure 8-61. CMD# Pulse Width (All)—t23b

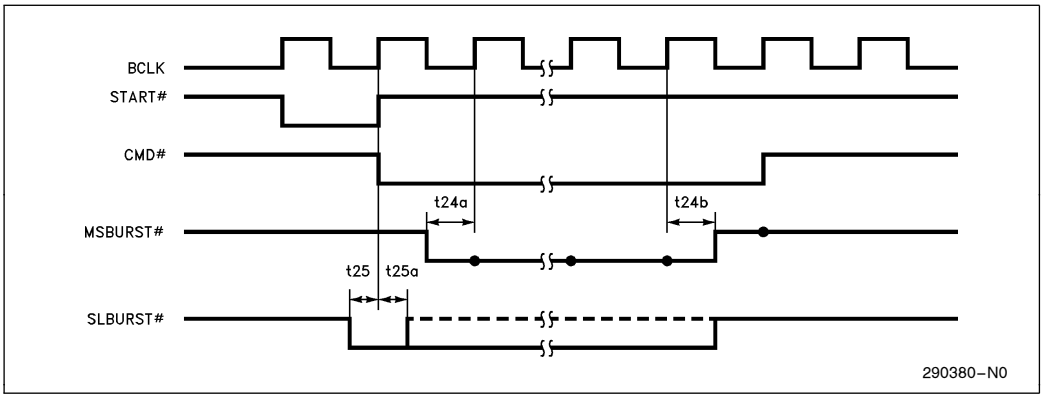


Figure 8-62. EISA Master Burst Cycle—t24a, t24b, t25, t25a

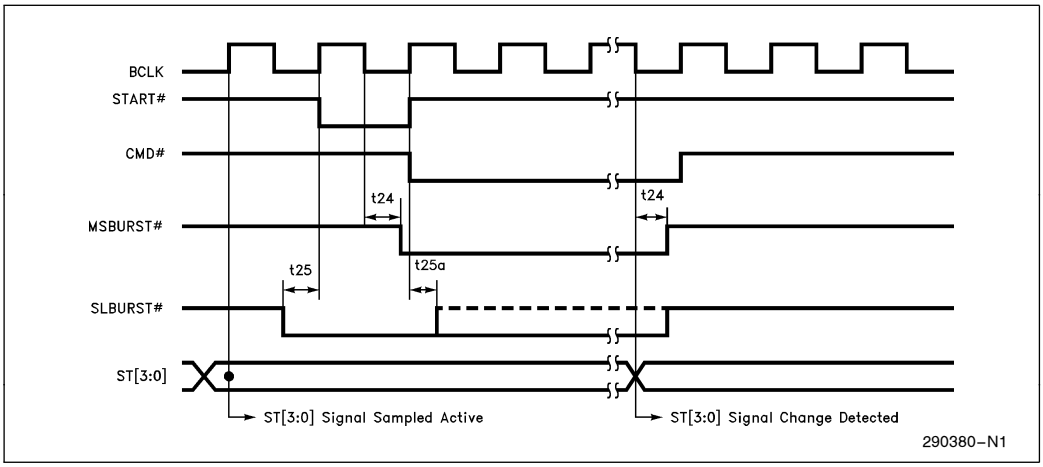


Figure 8-63. DMA Master Burst Cycle—t24, t25, t25a

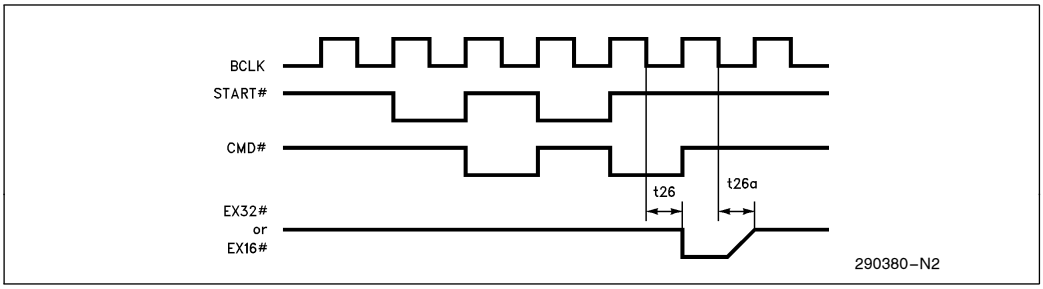


Figure 8-64. EISA Master Back-Off Cycle—t26, t26a

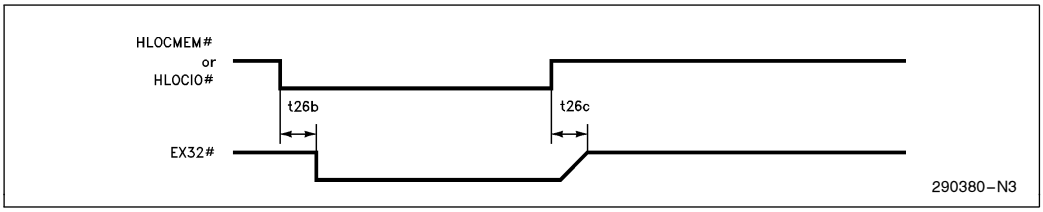


Figure 8-65. EISA Master to Host Slave Cycle—t26b, t26c

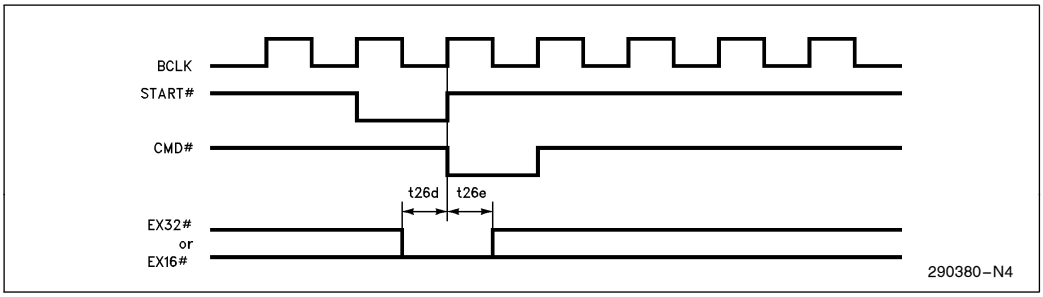


Figure 8-66. HOST, EISA, or DMA Master Cycle—t26d, t26e

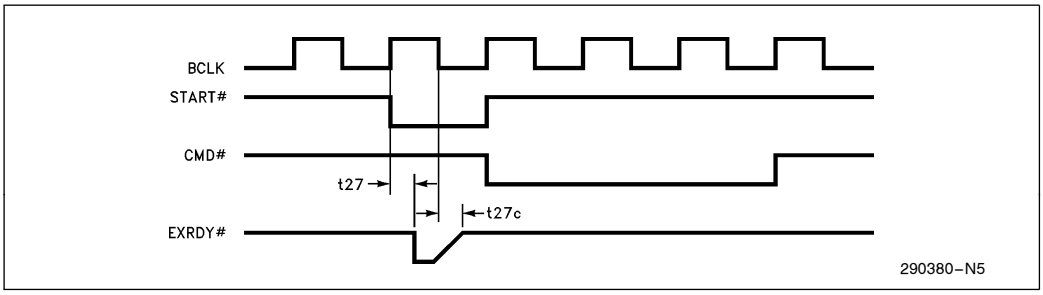


Figure 8-67. DMA Master Burst Write Cycle—t27, t27c

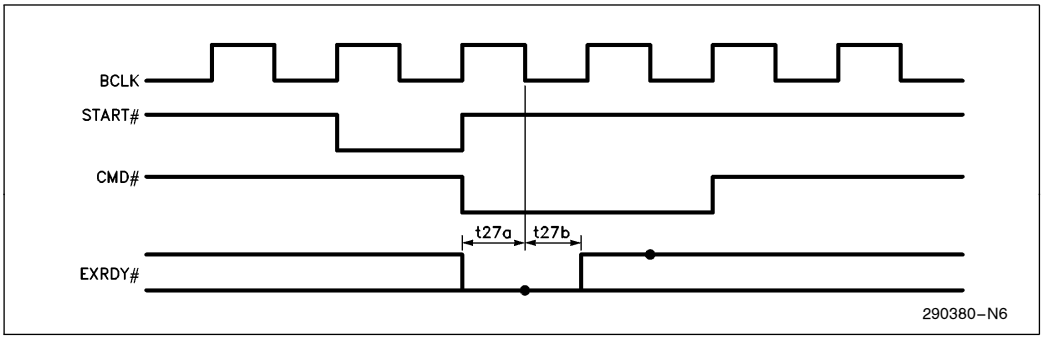


Figure 8-68. EXRDY Setup and Hold Timing (All)—t27a, t27b

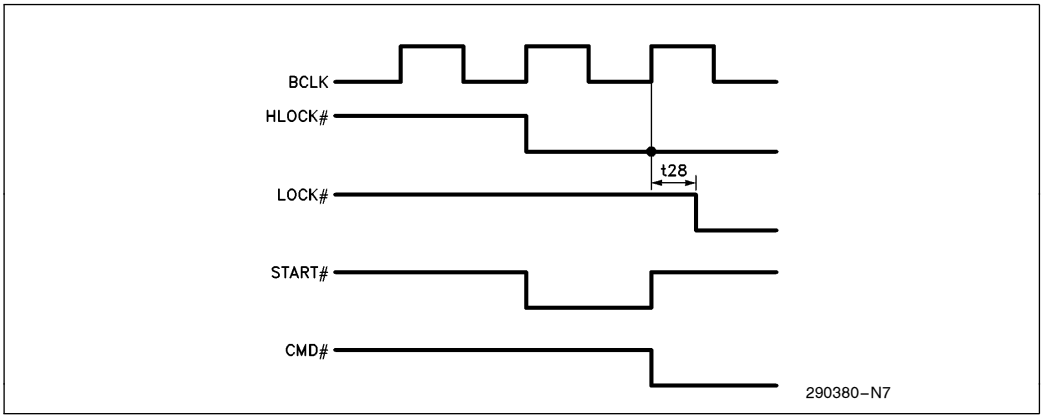


Figure 8-69. First Cycle of a LOCK—t28

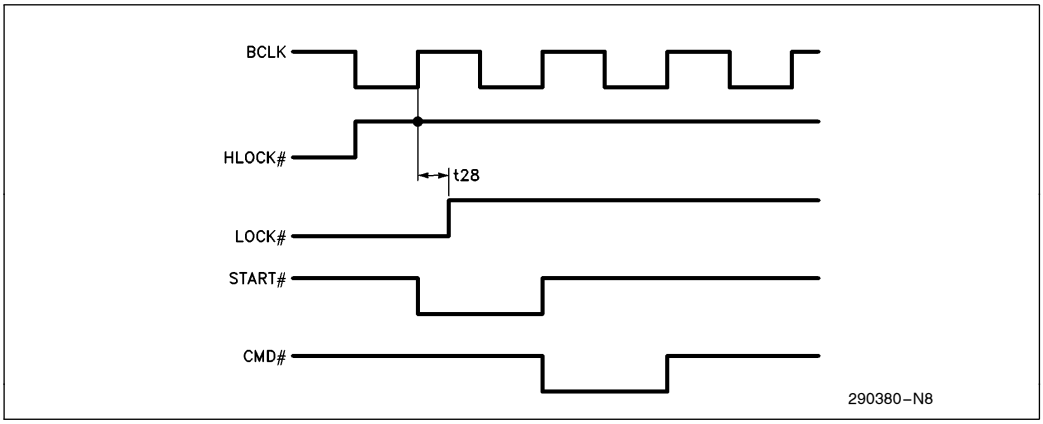


Figure 8-70. End of LOCK Where HLOCK# is Sampled Inactive on the Following Cycles START#—t28

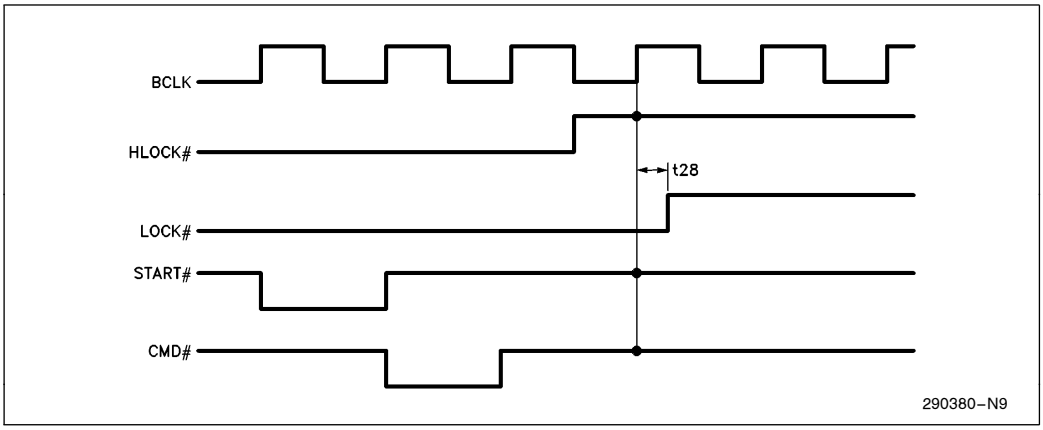


Figure 8-71. End of LOCK Where HLOCK#, START#, and CMD# are Sampled Inactive on the Rising Edge BCLK—t28

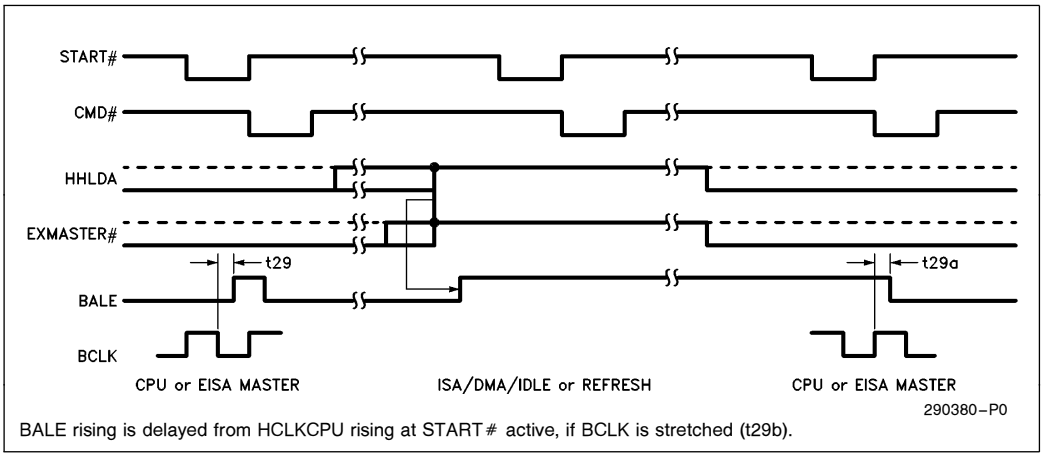


Figure 8-72. Bale Valid Delay—t29, t29a, t29b

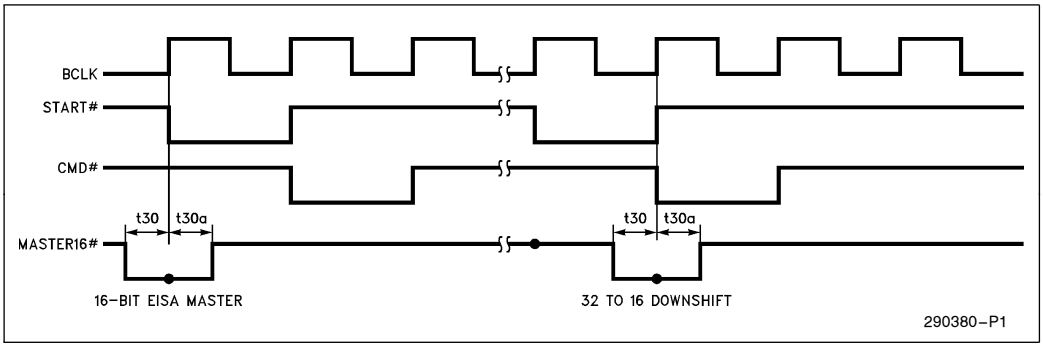


Figure 8-73. 16-Bit EISA Master or 32-Bit Downshifting Master Cycle—t30, t30a

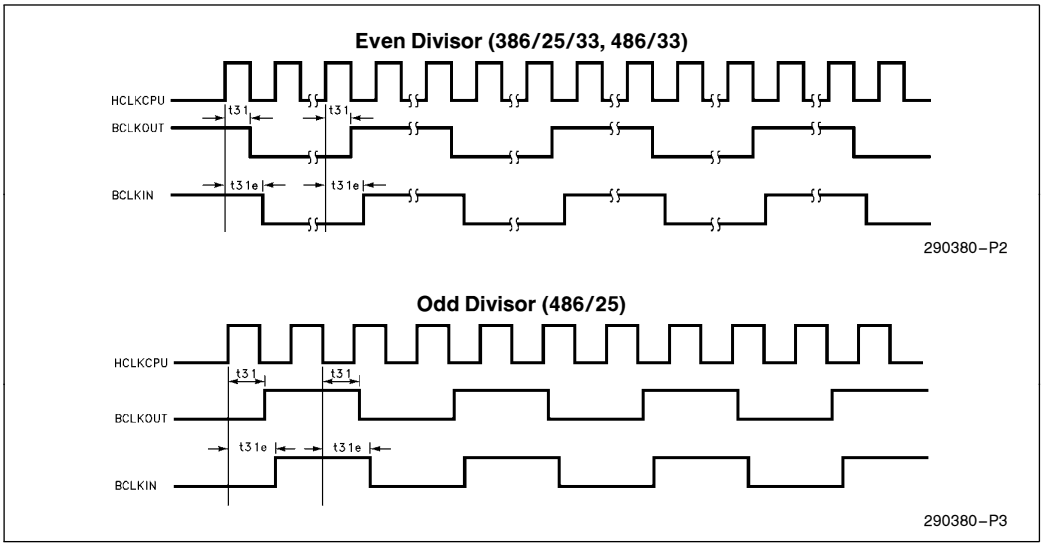


Figure 8-74. BCLK Valid Delay—t31

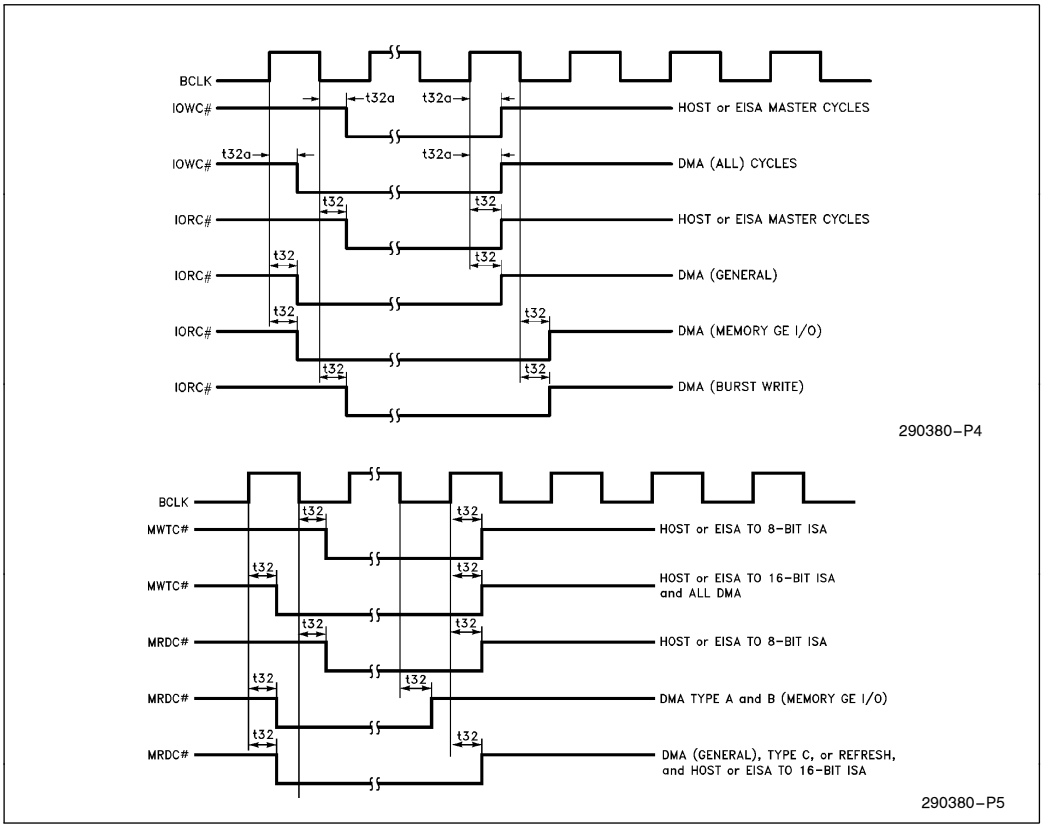


Figure 8-75. IORC#, IOWC#, MRDC#, and MWTC# Valid Delays—t32, t32a

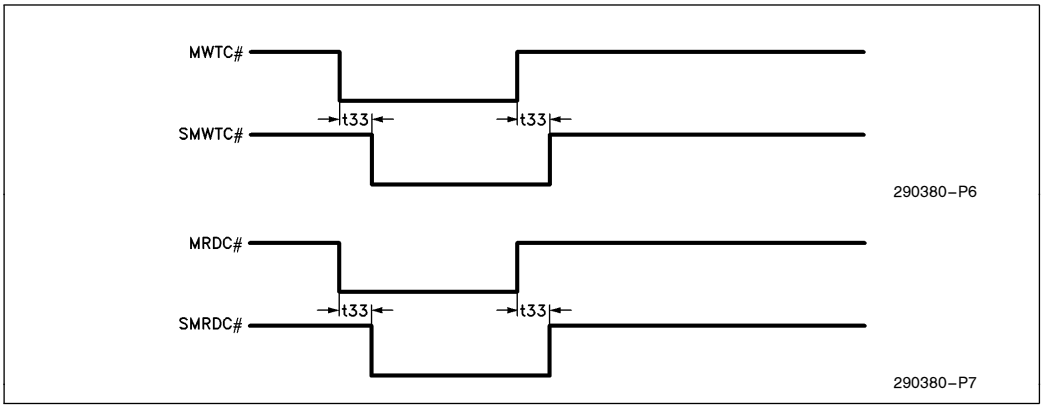


Figure 8-76. ISA Master Cycle Where the Addressed ISA Slave is within the 0 to 1 Mbyte Address Range—t33

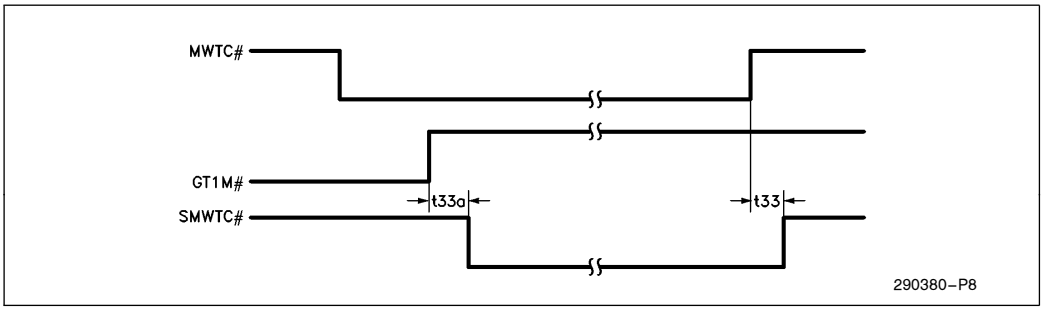


Figure 8-77. ISA Master Cycle Where GT1M# Decode Happens after the Assertion of MRDC# or MWTC#—t33, t33a

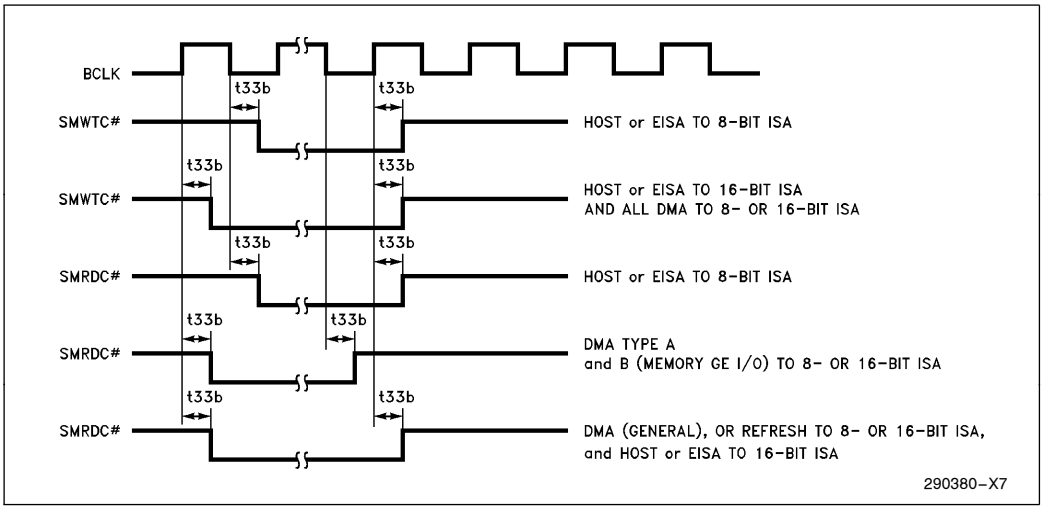


Figure 8-78. Non-ISA Master Cycle Where the Addressed ISA Memory Slave is within the 0 to 1 Mbyte Address Range

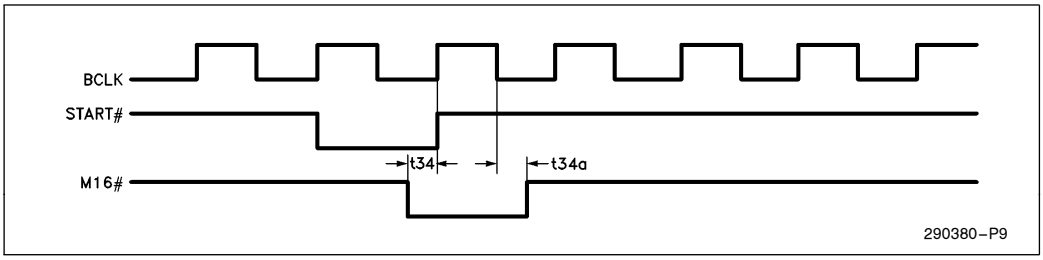


Figure 8-79. HOST, EISA, or DMA Master Cycle to ISA Memory—t34, t34a

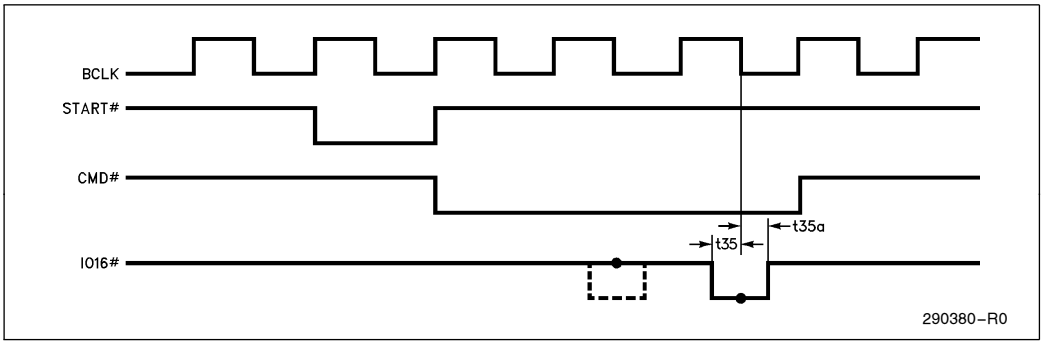


Figure 8-80. HOST or EISA Master Cycle to ISA I/O—t35, t35a

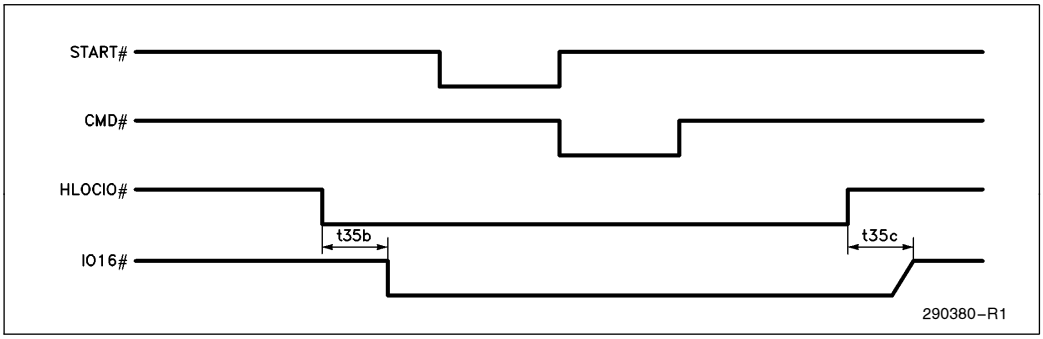
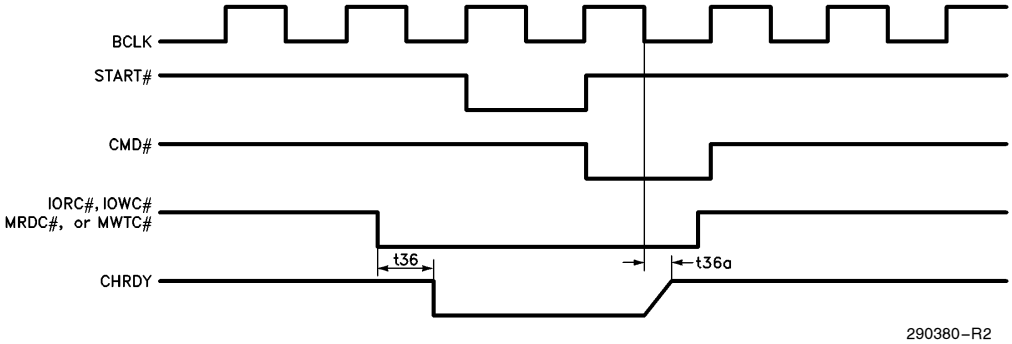


Figure 8-81. ISA Master to a Host I/O Slave—t35b, t35c



If either EXRDY or DRDY is sampled inactive, CHRDY will float from the falling edge of BCLK that EXRDY and DRDY are sampled active again.

Figure 8-82. ISA Master to EISA or Host Slave—t36, t36a

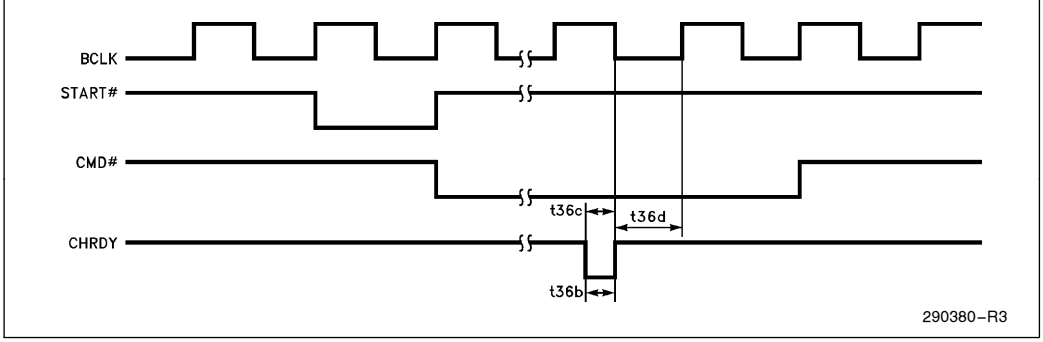


Figure 8-83. HOST, EISA or DMA Master to an ISA Slave (One Wait-State)—t36b, t36c, t36d

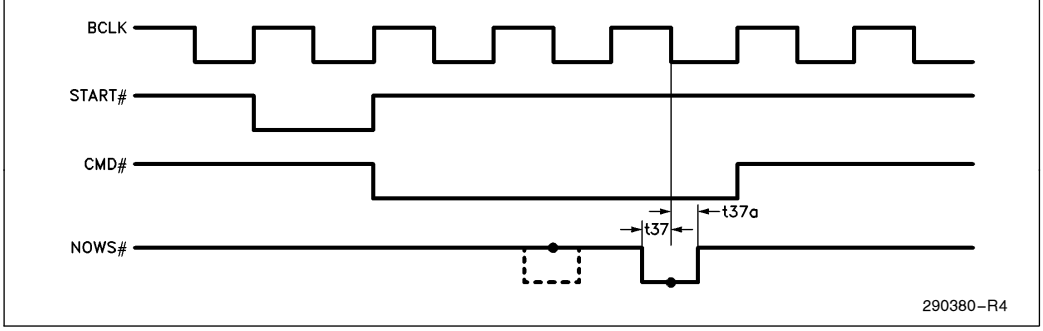


Figure 8-84. HOST or EISA Master Cycle to an 8-Bit ISA Slave—t37, t37a

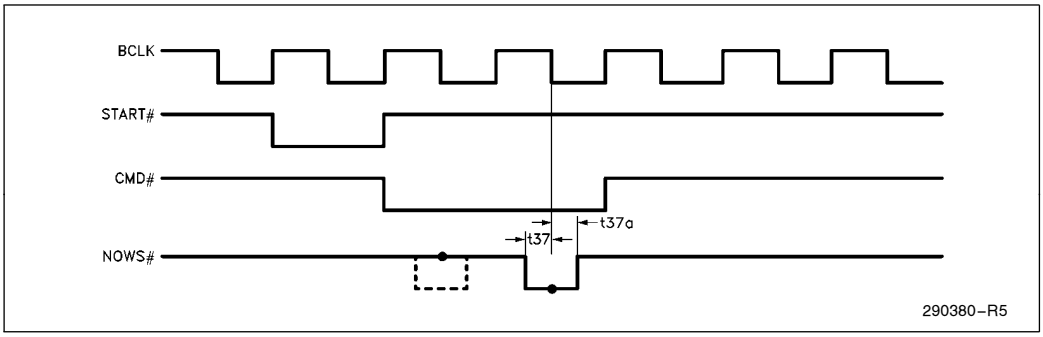
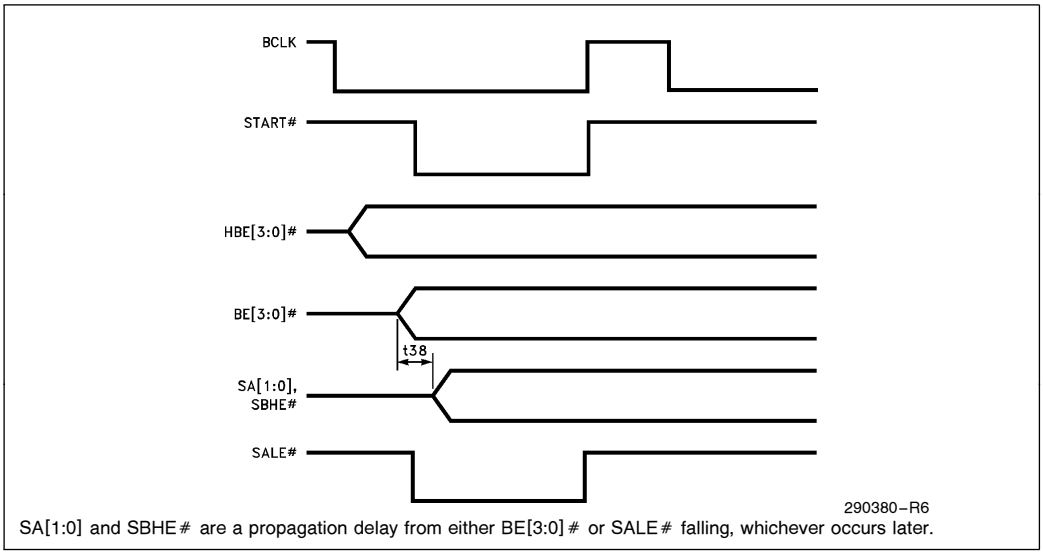


Figure 8-85. HOST or EISA Master Cycle to a 16-Bit ISA Slave—t37, t37a



SA[1:0] and SBHE# are a propagation delay from either BE[3:0]# or SALE# falling, whichever occurs later.

Figure 8-86. Host Master Cycle (with BCLK Stretching)—t38

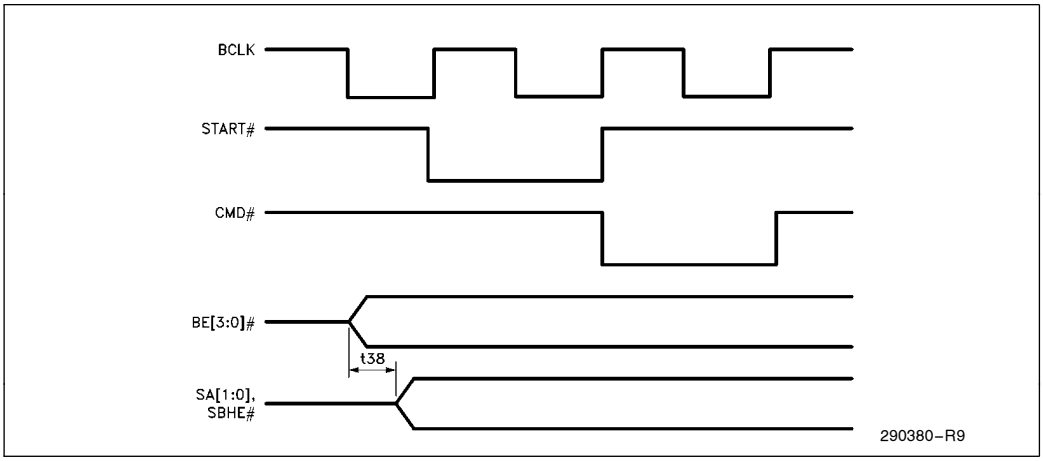


Figure 8-87. DMA or REFRESH Master Cycle—t38

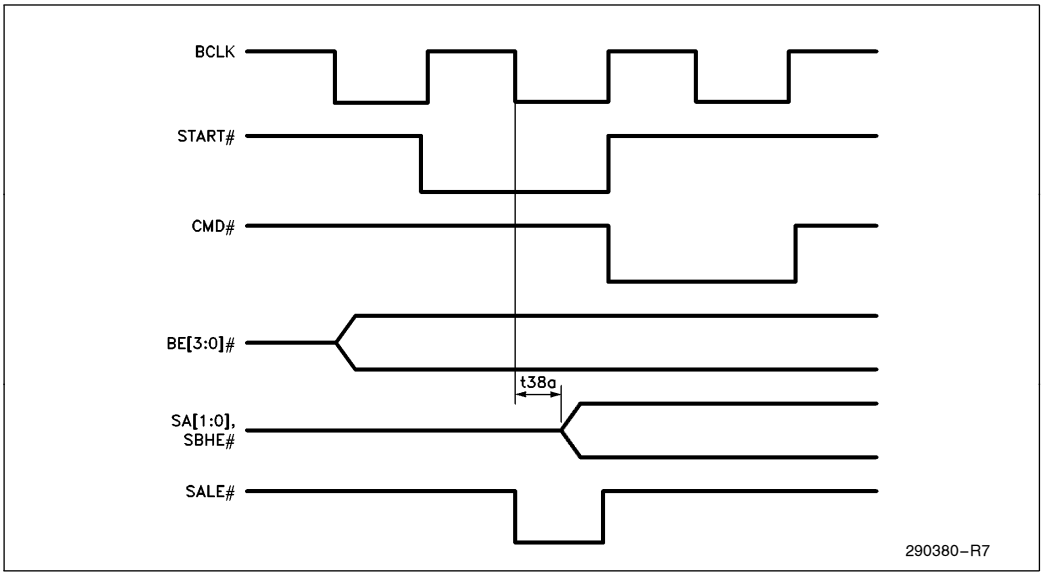


Figure 8-88. EISA Master Cycle—t38a

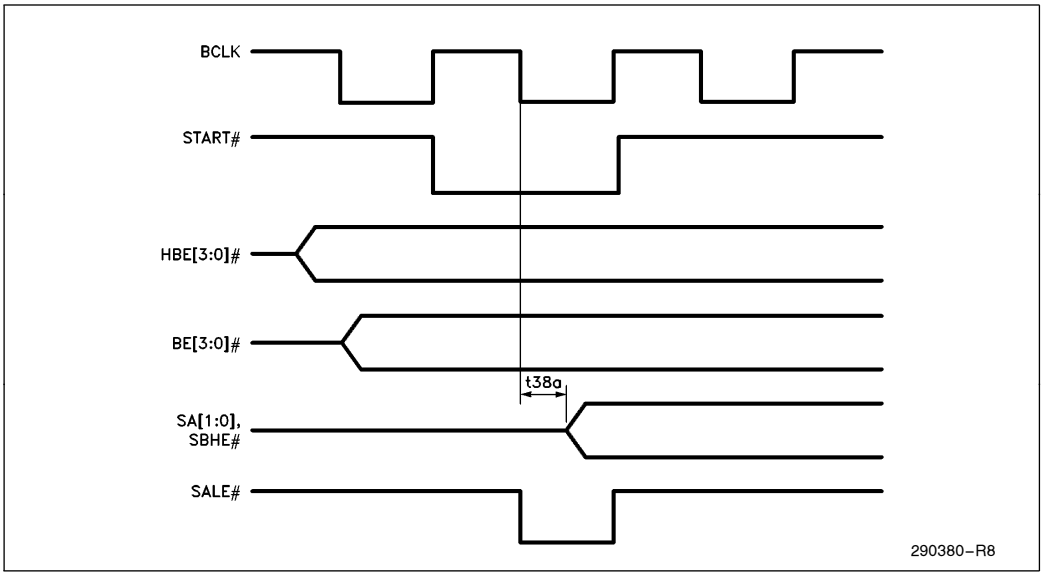


Figure 8-89. Host Master Cycle (without BCLK Stretching)—t38a

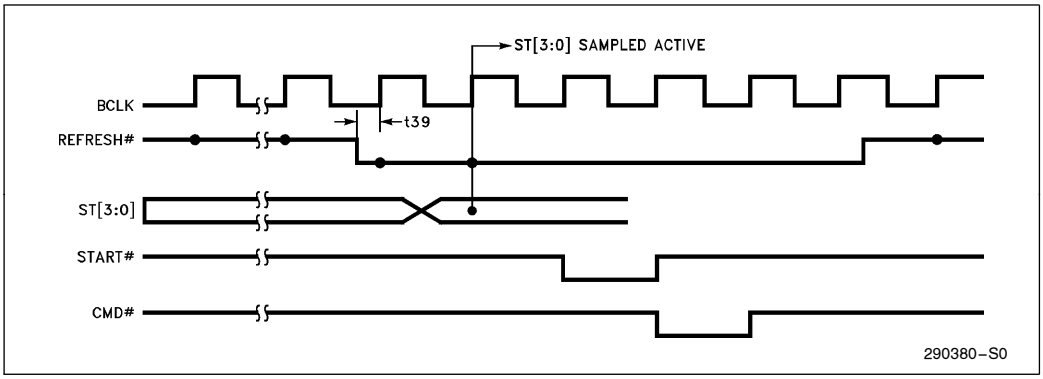


Figure 8-90. 82357 (ISP) Initiated Refresh—t39

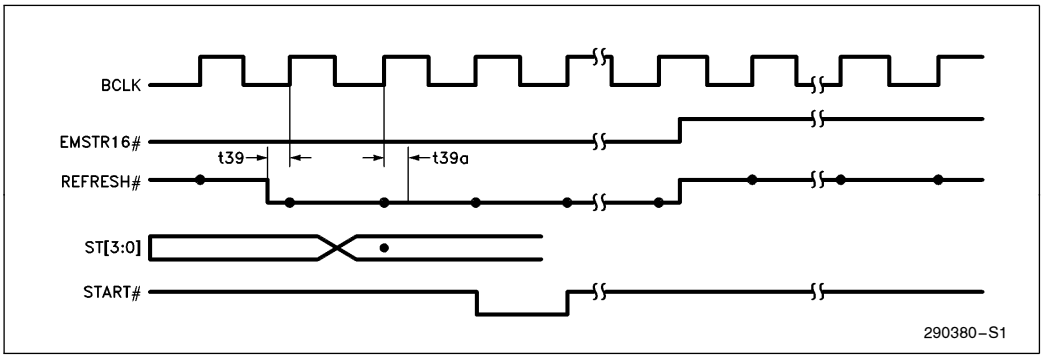


Figure 8-91. ISA Master Initiated Refresh—t39, t39a

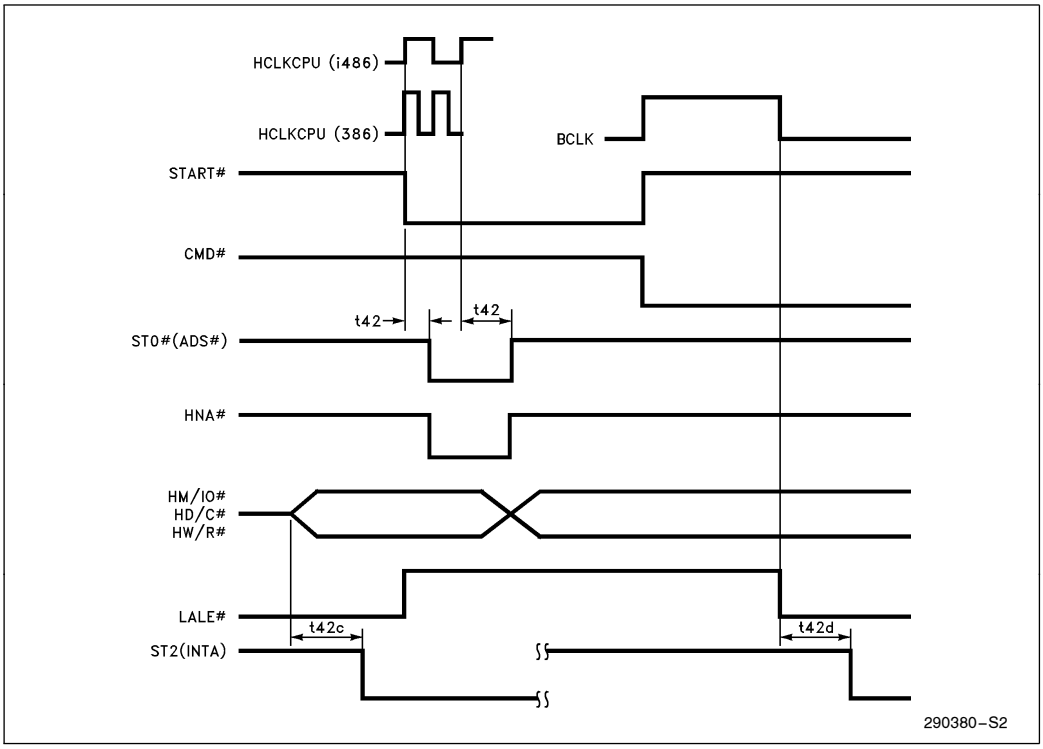


Figure 8-92. Host Master Cycle to the 82357 (ISP)—t42, t42c, t42d

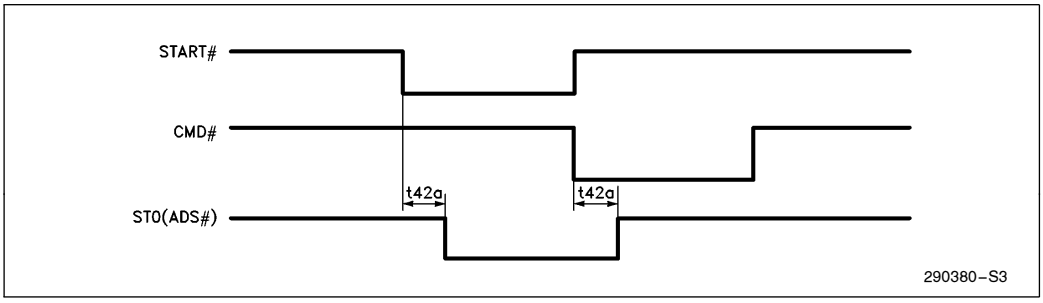


Figure 8-93. EISA Master Cycle to the 82357 (ISP)—t42a

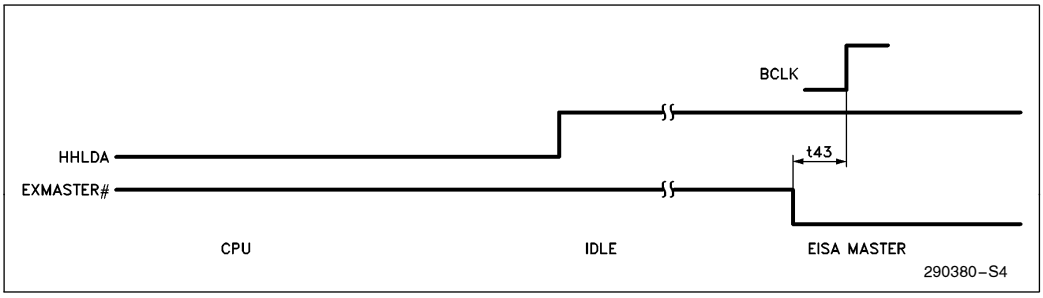


Figure 8-94. EISA Master Cycle—t43

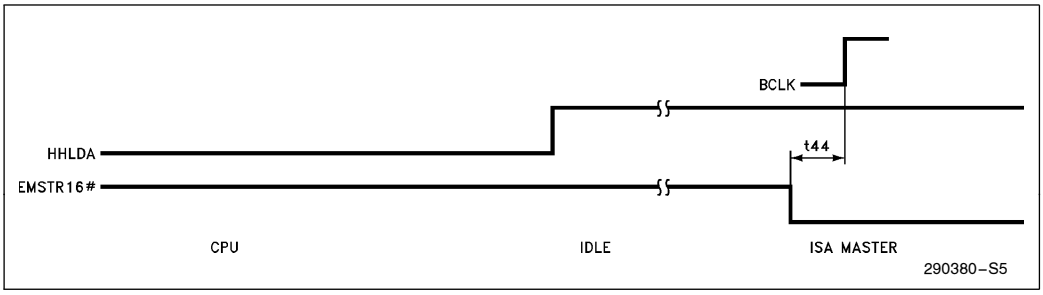


Figure 8-95. ISA Master Cycle—t44

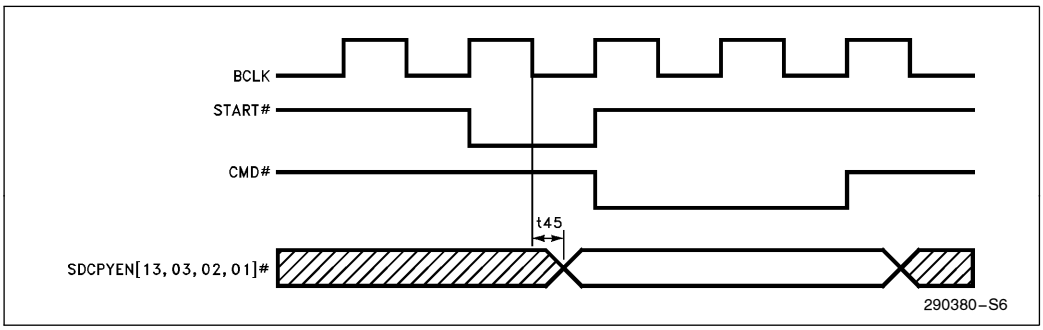
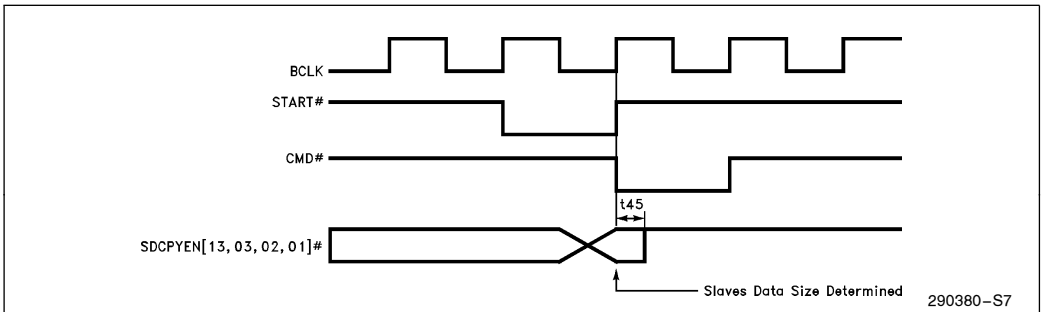


Figure 8-96. HOST, EISA, ISA (to EISA I/O), or DMA Write Cycle—t45 (Active Edge)



Before the slaves size is determined, copying is done assuming a default slave size as follows: (16-bit slave for a 32-bit master, and a 32-bit slave for a 16-bit master). If a match is determined, the copy enable signals are driven inactive on the rising edge of BCLK that START# is driven inactive.

Figure 8-97. 32-Bit or 16-Bit EISA or DMA Master Write Cycle Where the Master and Slave Data Size is Matched (e.g., 32-Bit Master/32-Bit Slave)—t45

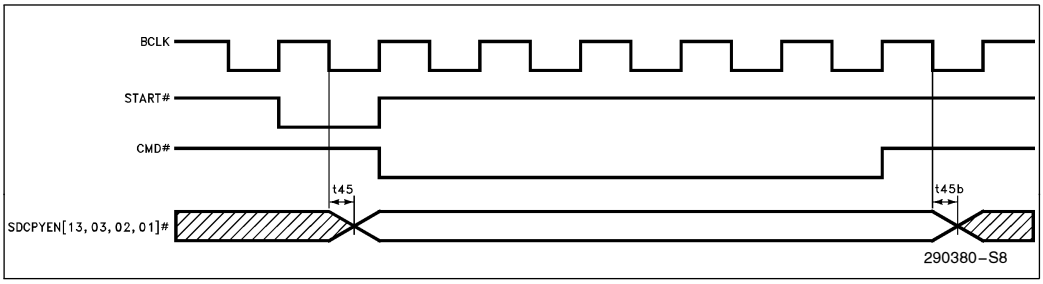


Figure 8-98. EISA Master or DMA Burst Write Cycle—t45 (Active Edge), t45b (Inactive Edge)

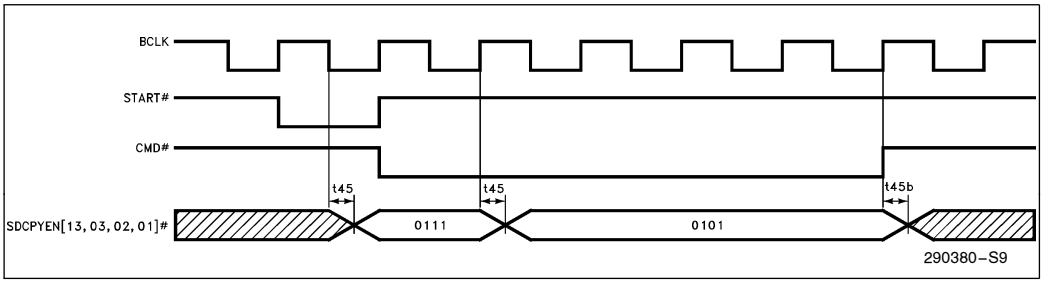
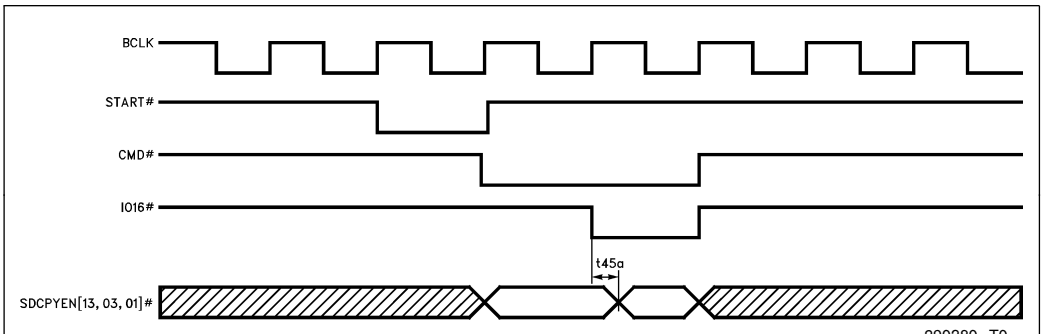


Figure 8-99. EISA Master or DMA Burst Write Cycle Where the Masters Data Size Is Less Than the Slaves Data Size and the Initial Transfer is Misaligned (e.g., Initial BE[3:0]# = 0111)—t45 (Active Edge), t45b (Inactive Edge)



SDCPYEN02# is not delayed from the falling edge of IO16#. The 82358DT treats SDCPYEN02# the same for 8-bit slave devices and 16-bit slave devices. If SDCPYEN02# is inactive coming into the cycle, it will be driven active on the rising edge of BCLK at START# driven inactive.

Figure 8-100. HOST, EISA, or DMA Master Read Cycle from a 16-Bit ISA I/O—t45a (Active/Inactive Edges)

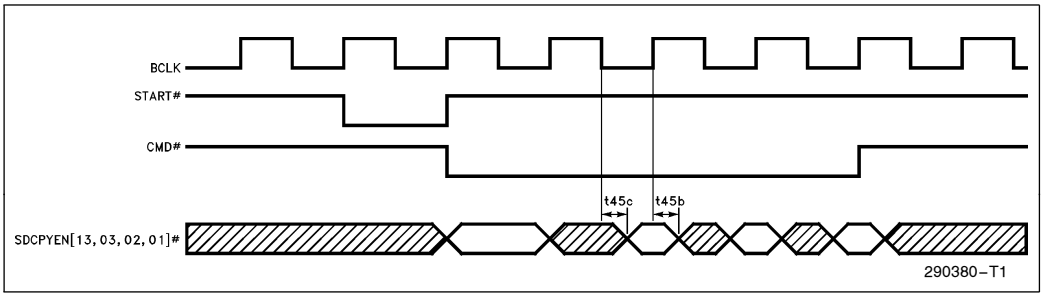


Figure 8-101. EISA Master or DMA Burst Read Cycle—t45b (Inactive Edge), t45c (Active Edge)

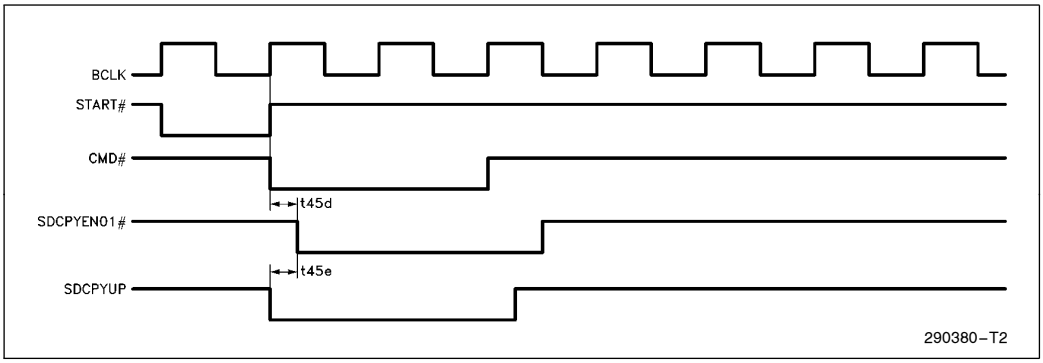


Figure 8-102. 16-Bit EISA Master Write to an 8-Bit EISA/ISA Slave (BE# = 1101)—t45d, t45e

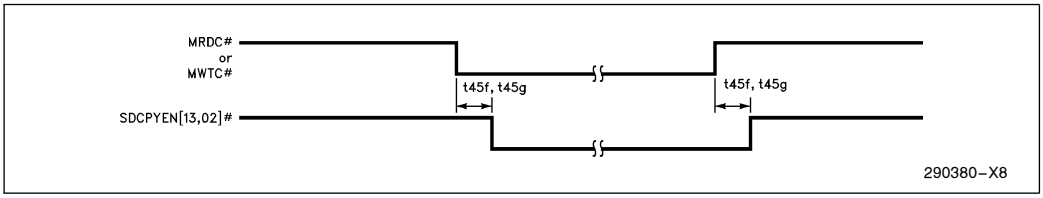


Figure 8-103. ISA Master to Host Memory That Supports ISA Cycles—t45f, t45g

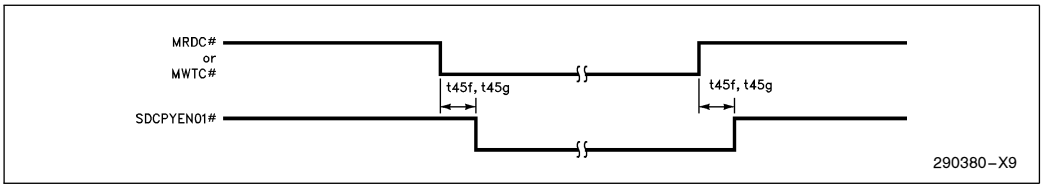


Figure 8-104. ISA Master to 8-Bit Memory—t45f, t45g

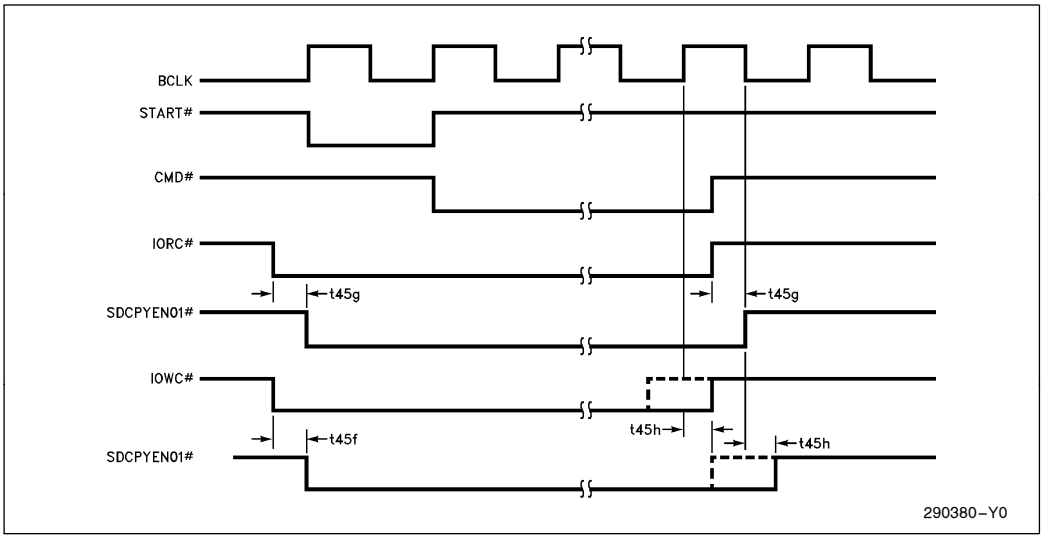


Figure 8-105. ISA Master to 8-Bit I/O—t45f, t45g, t45h

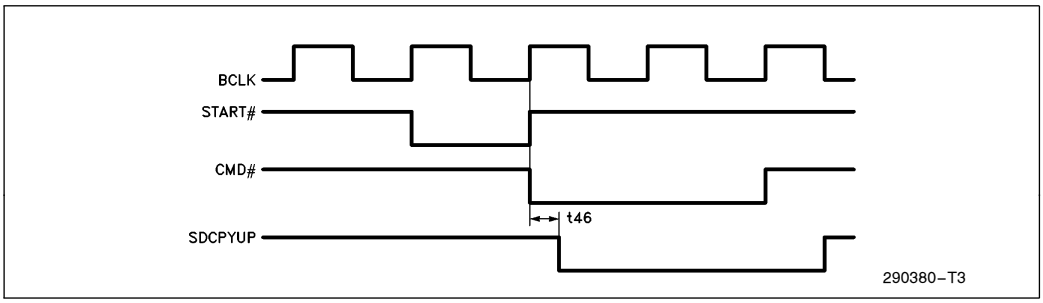


Figure 8-106. 16-Bit EISA or DMA Master Write Cycle to an 8-Bit ISA Slave (BE# = 0111, 1101)—t46

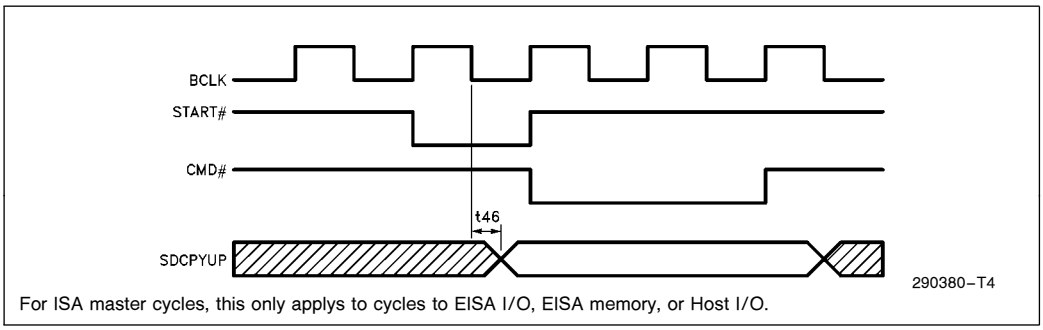


Figure 8-107. HOST, EISA, ISA, or DMA Master Write Cycle—t46

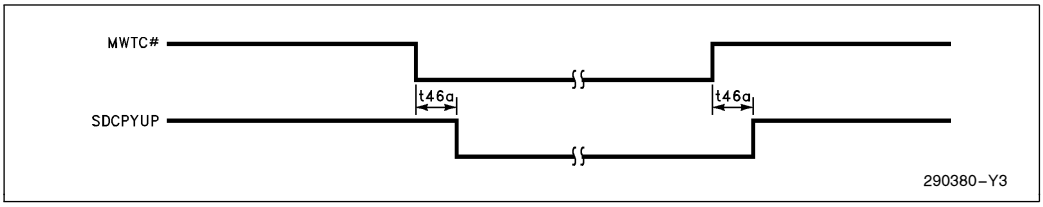


Figure 8-108. ISA Master Write to 8-Bit Memory—t46a

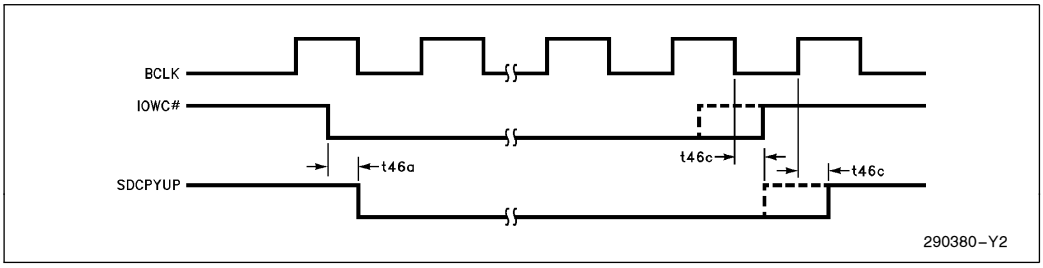


Figure 8-109. ISA Master Write to 8-Bit ISA I/O—t46a, t46c

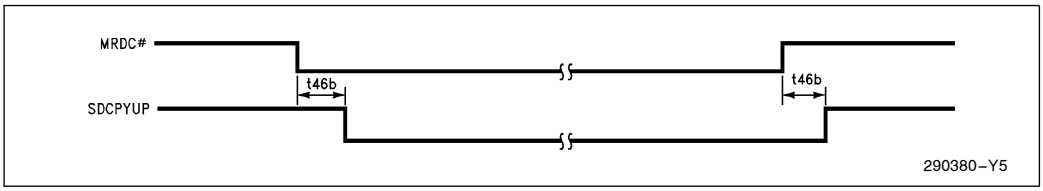


Figure 8-110. ISA Master Read from Host Memory—t46b

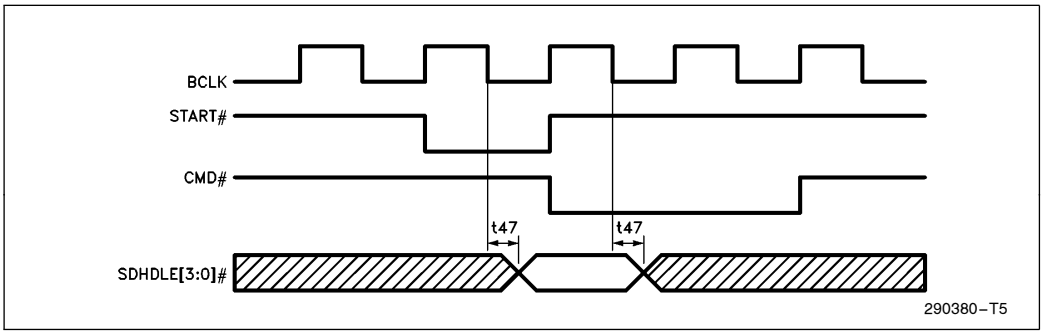


Figure 8-111. EISA, or DMA Master Write Cycle—t47

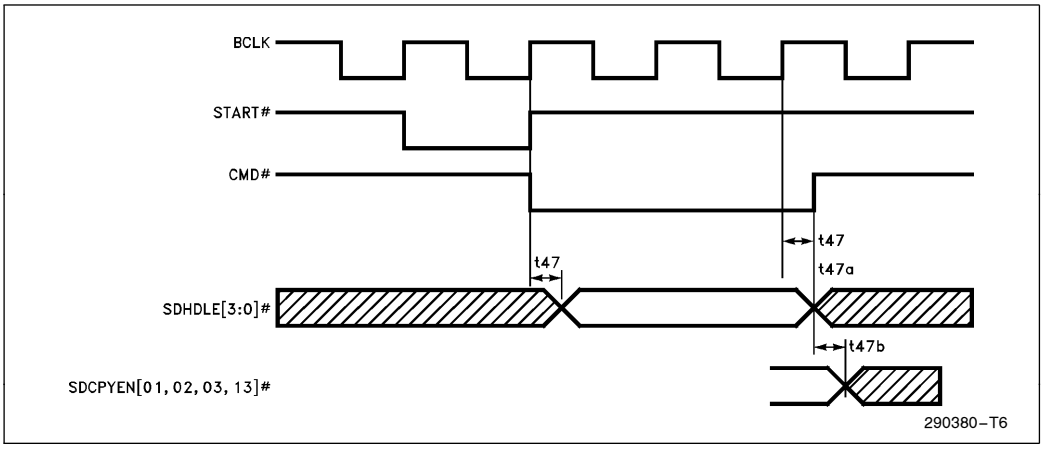


Figure 8-112. HOST, EISA (Non-Burst), or DMA (Non-Burst) Master Read Cycle—t47, t47a, t47b

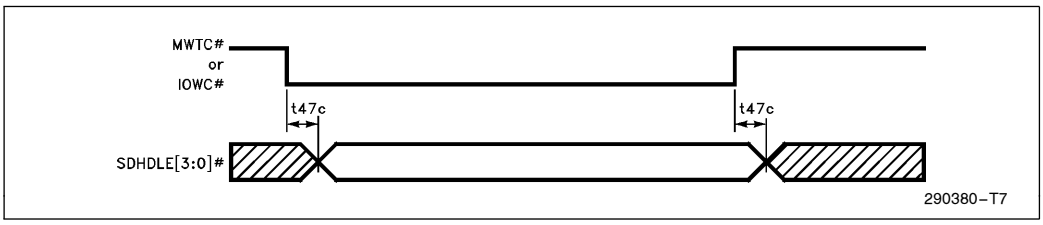


Figure 8-113. ISA Master Write Cycle—t47c

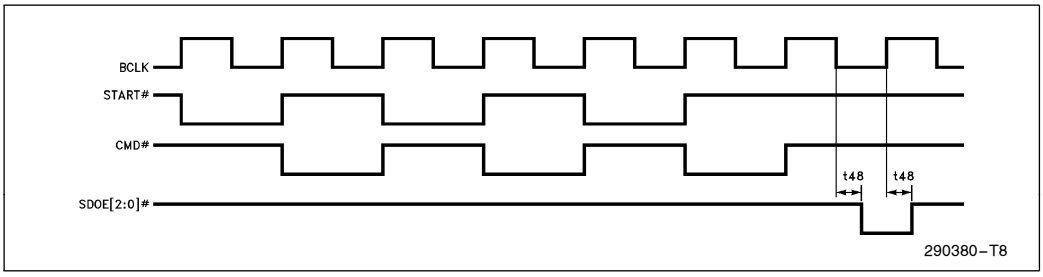


Figure 8-114. EISA Master Read Re-Drive Cycle—t48

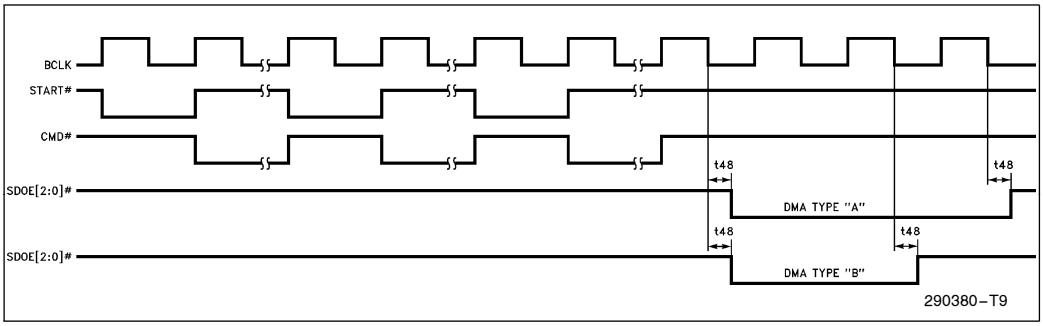


Figure 8-115. DMA Master Read Re-Drive Cycle—t48

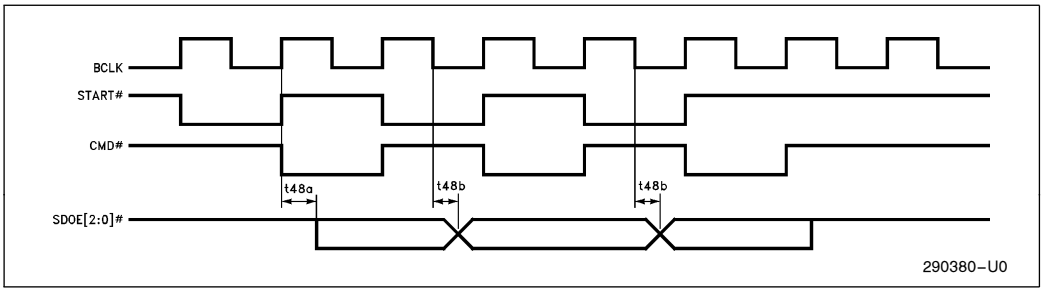
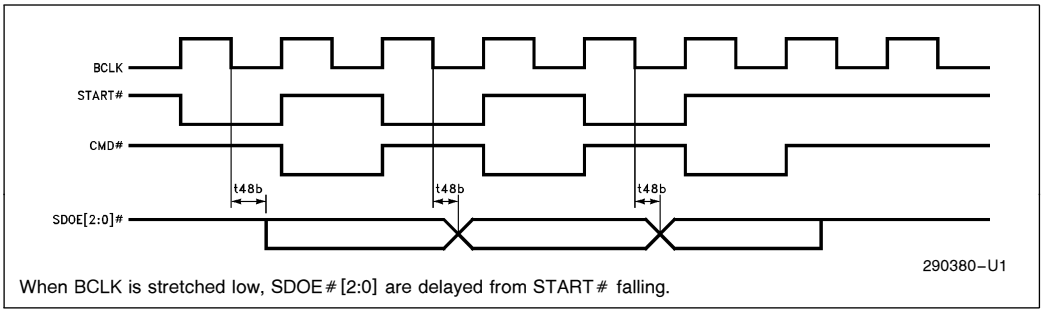


Figure 8-116. EISA Master Disassembly Cycle—t48a, t48b



When BCLK is stretched low, SDOE# [2:0] are delayed from START# falling.

Figure 8-117. Host Master to the EISA/ISA Bus Disassembly Cycle—t48b

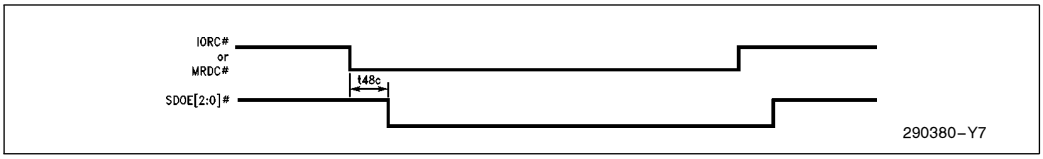


Figure 8-118. ISA Master Read from a Host Slave—t48c

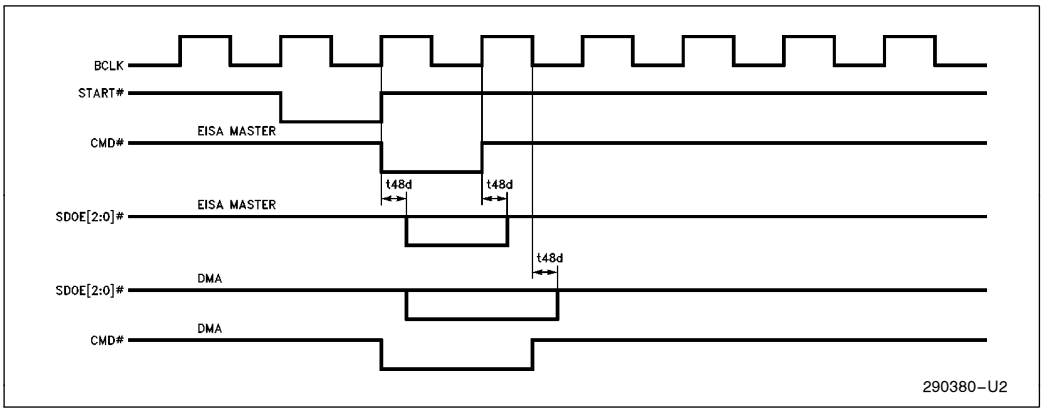


Figure 8-119. EISA or DMA Master Read from a Host Slave—t48d

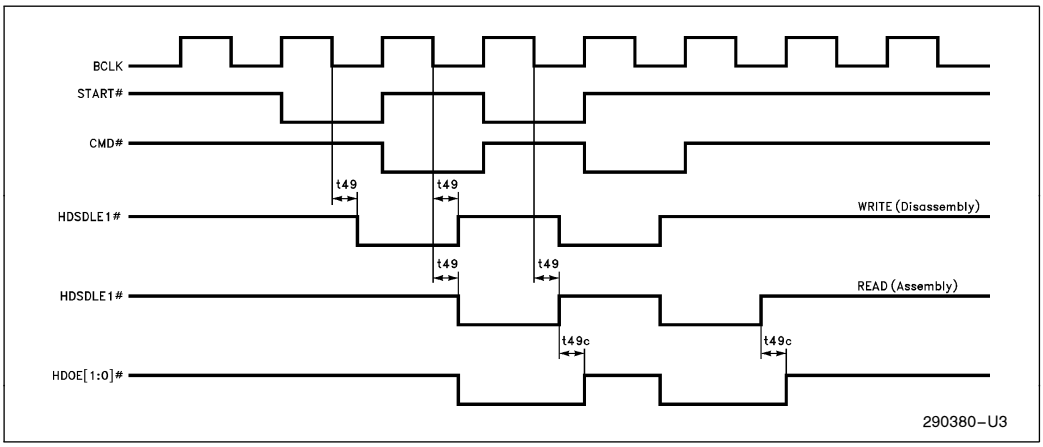


Figure 8-120. EISA Master Re-Drive Cycle—t49, t49c

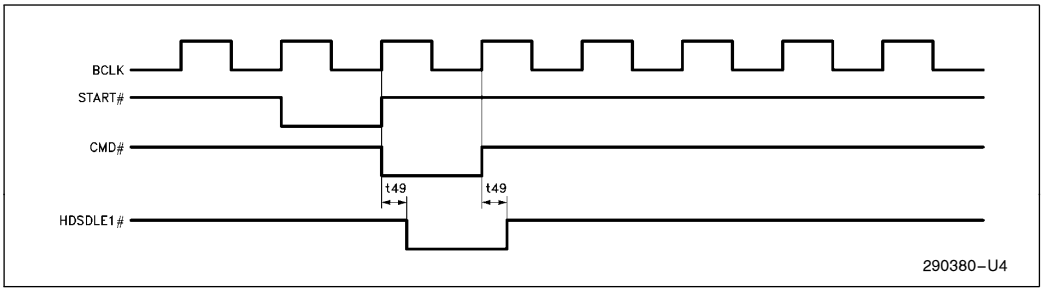


Figure 8-121. EISA or DMA Master Read Cycle from a Host Slave—t49

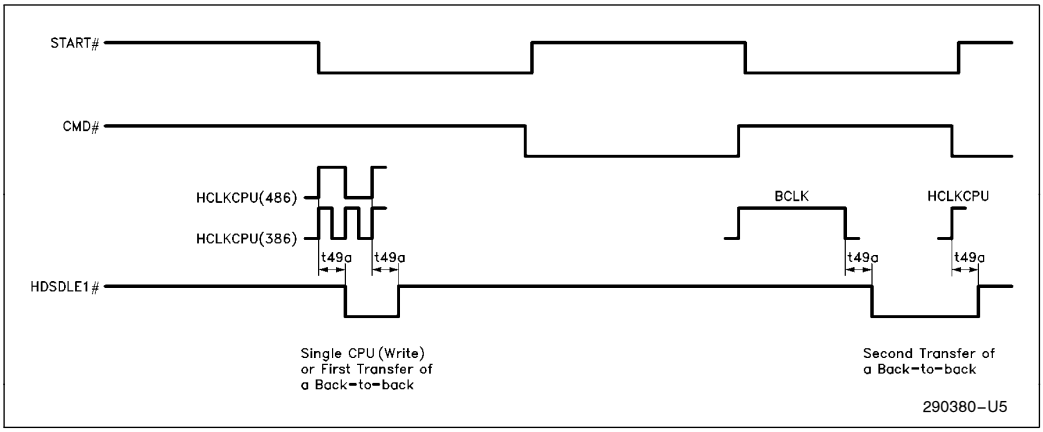


Figure 8-122. Host Master Write Cycle to the EISA/ISA Bus—t49a

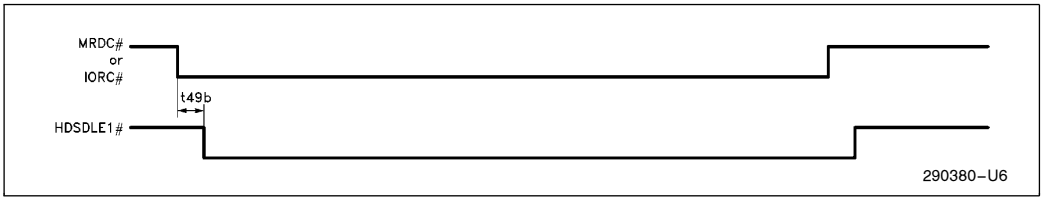
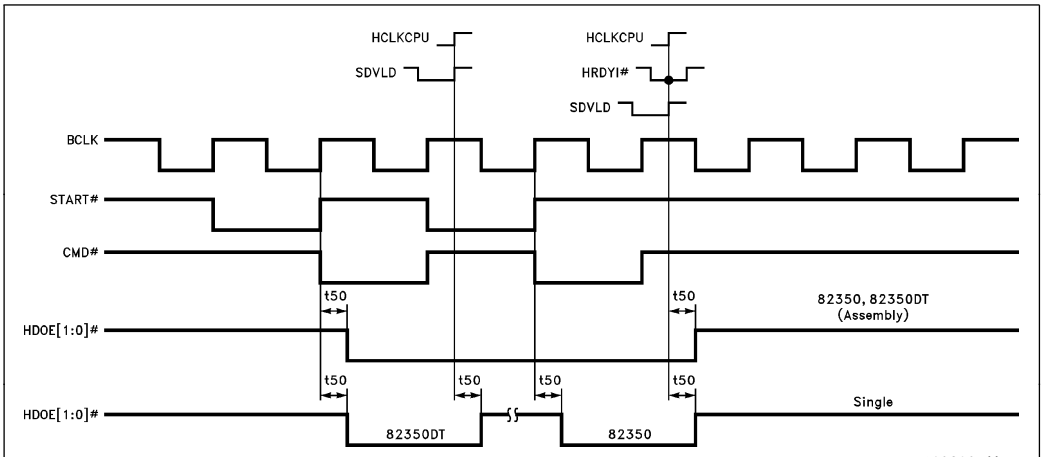


Figure 8-123. ISA Master Read Cycle (Active Edge Only)—t49b



In an 82350 system, HDOE[1:0]# are driven inactive from the rising edge of HCLKCPU where HRDYI# is sampled low.
In an 82350DT system, HDOE[1:0]# are driven inactive from the rising edge of HCLKCPU that SDVLD is driven high.

Figure 8-124. Host Master Read Cycle from the EISA/ISA Bus (Single or Assembly Cycle)—t50

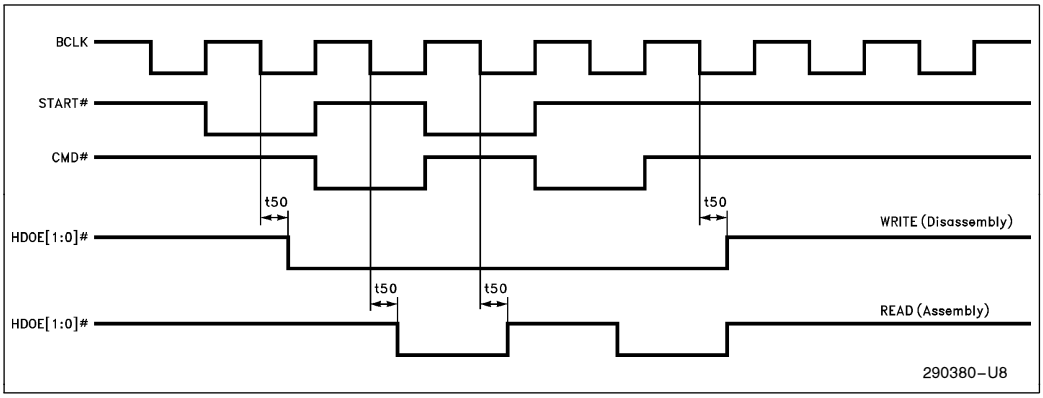


Figure 8-125. EISA Master Re-Drive Cycle—t50

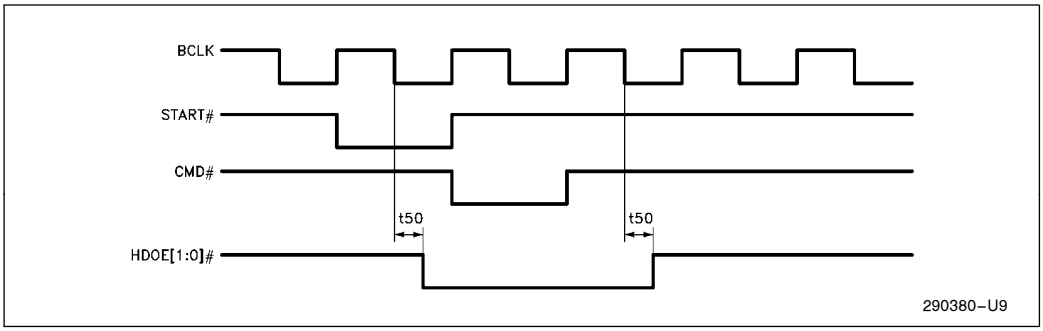


Figure 8-126. EISA or DMA Master Write Cycle to the Host Bus—t50

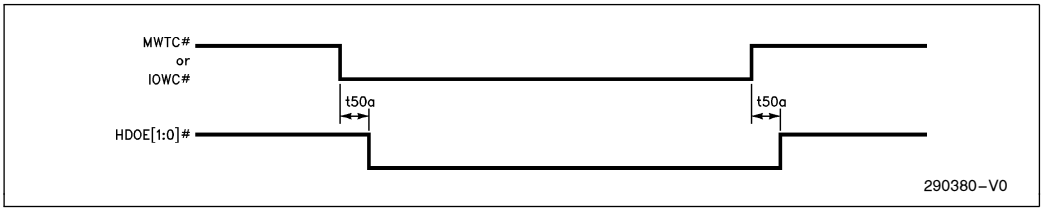


Figure 8-127. ISA Master Write Cycle—t50a

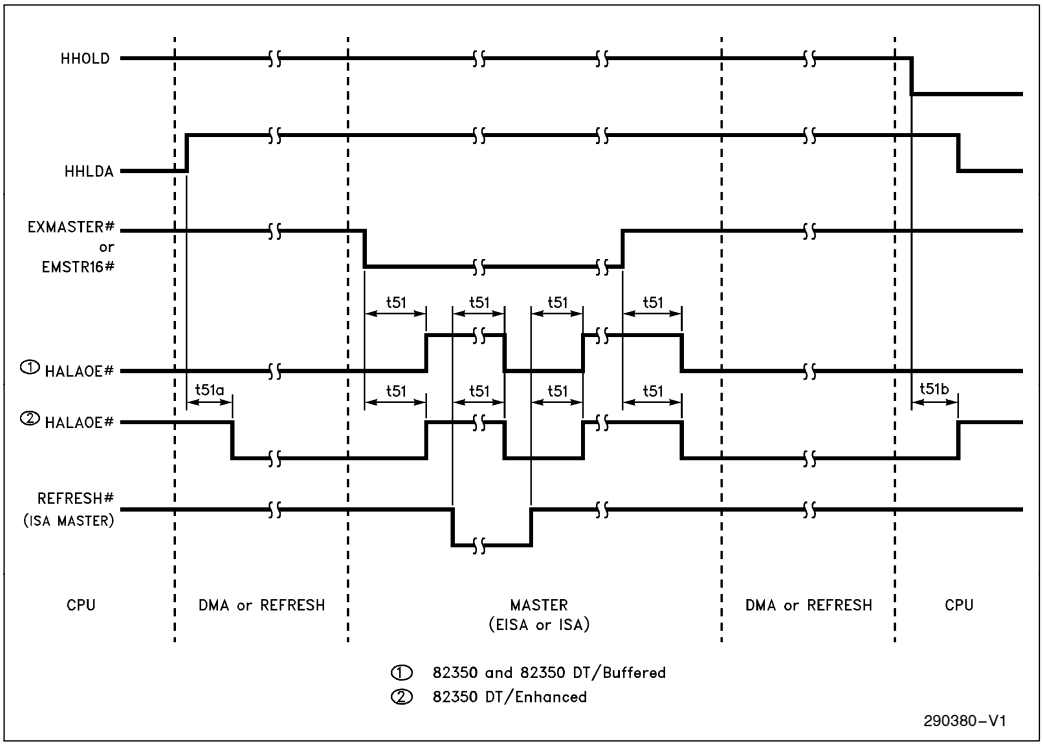


Figure 8-128. HOST, EISA, ISA, DMA, or Refresh Master Cycle—t51, t51a, t51b

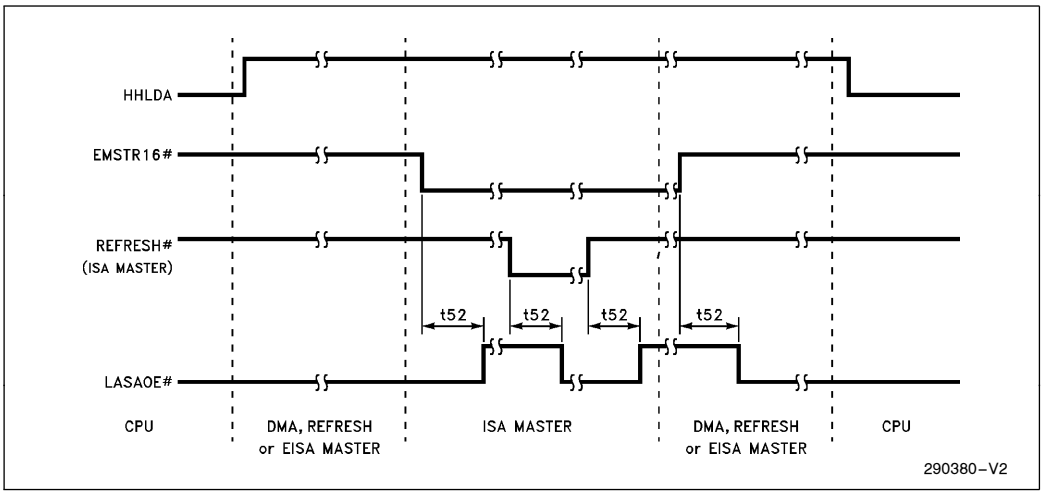


Figure 8-129. HOST, EISA, ISA, DMA, or Refresh Master Cycle—t52

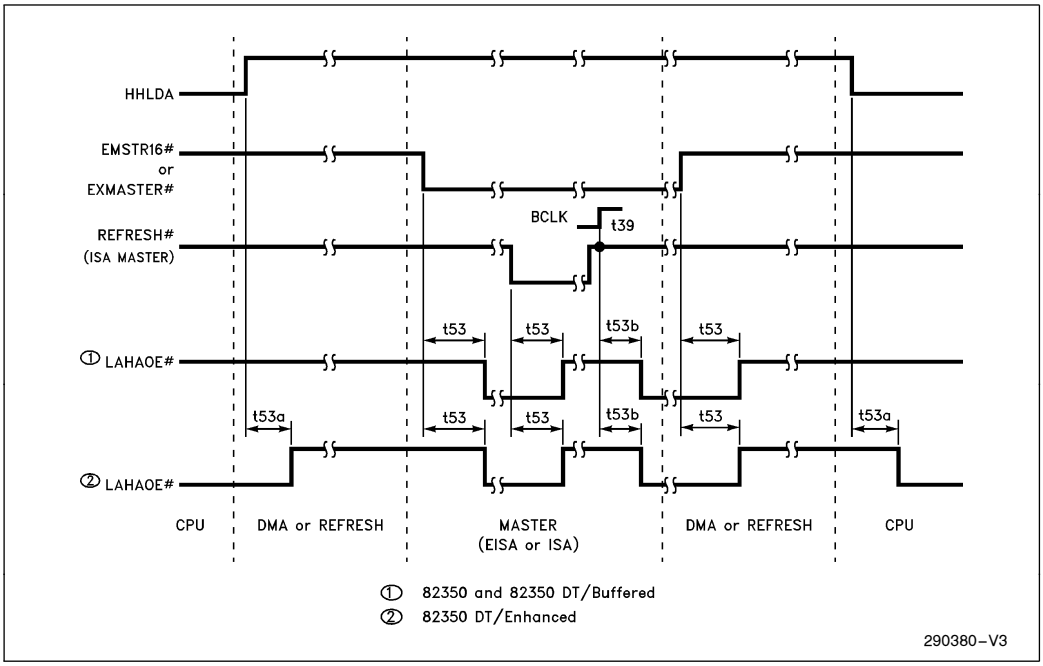


Figure 8-130. HOST, EISA, ISA, DMA, or Refresh Master Cycle—t53, t53a, t53b

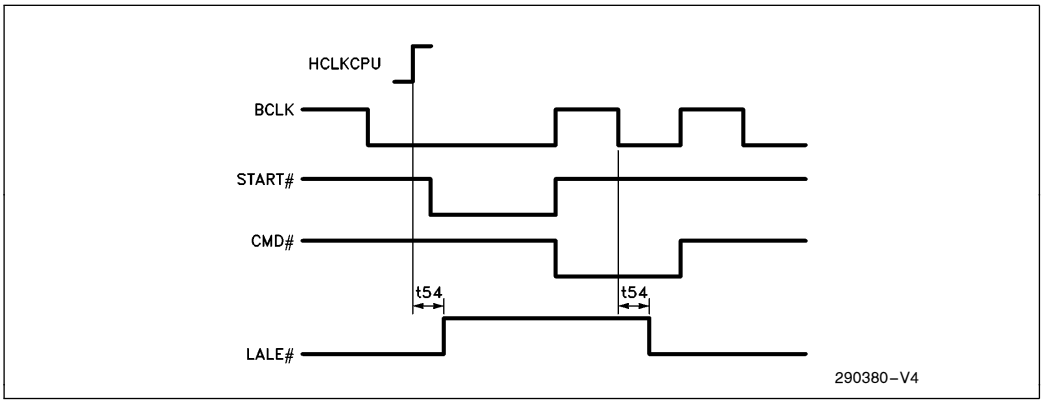


Figure 8-131. Host Master Cycle with BCLK Stretching—t54

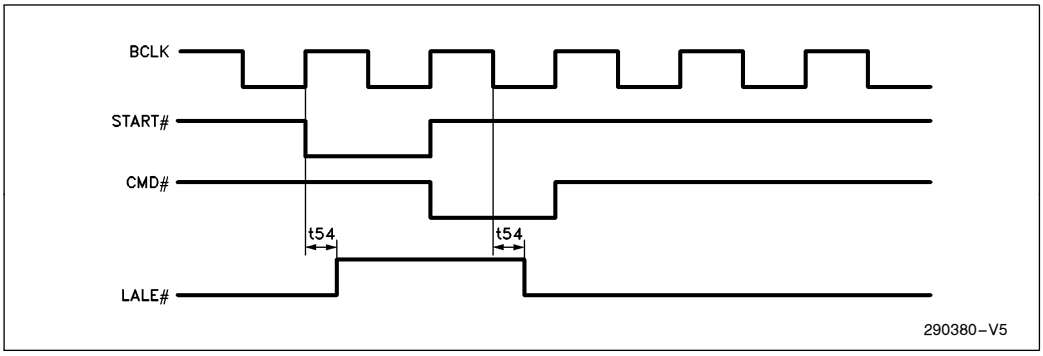


Figure 8-132. Host Master Cycle without BCLK Stretching—t54

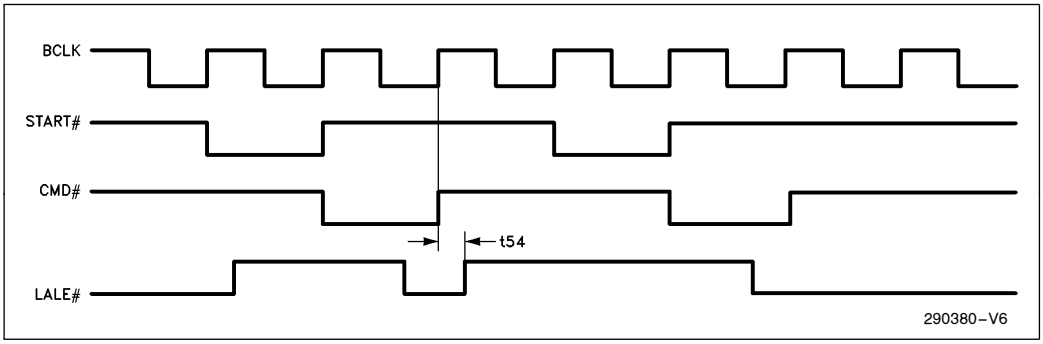


Figure 8-133. Host Master Cycle to an ISA I/O Slave (Pipelined)—t54

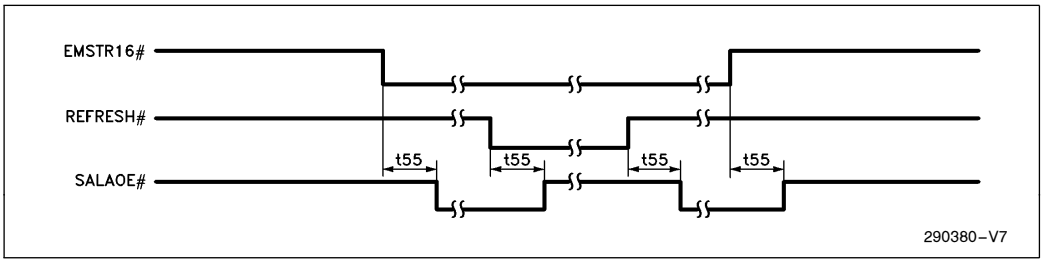


Figure 8-134. SALAOE# Propagation Delay (All)—t55

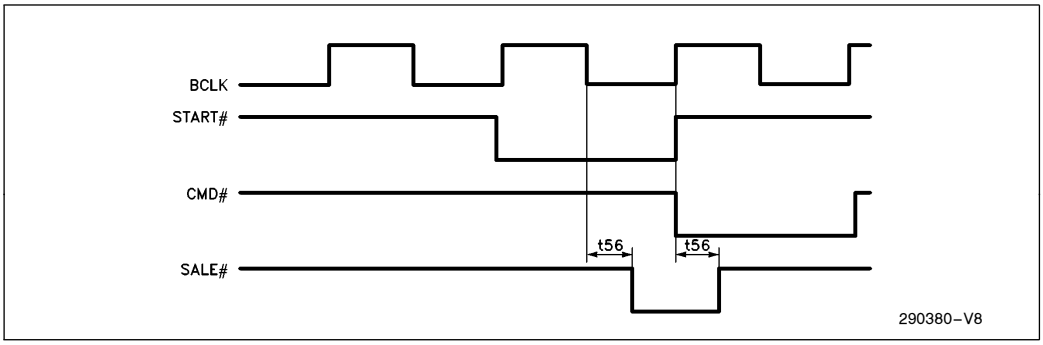


Figure 8-135. HOST, EISA, or DMA Master Cycle (Note: For DMA Cycles, This Only Applies to the Subsequent Cycle of an Assembly or Disassembly Cycle)—t56

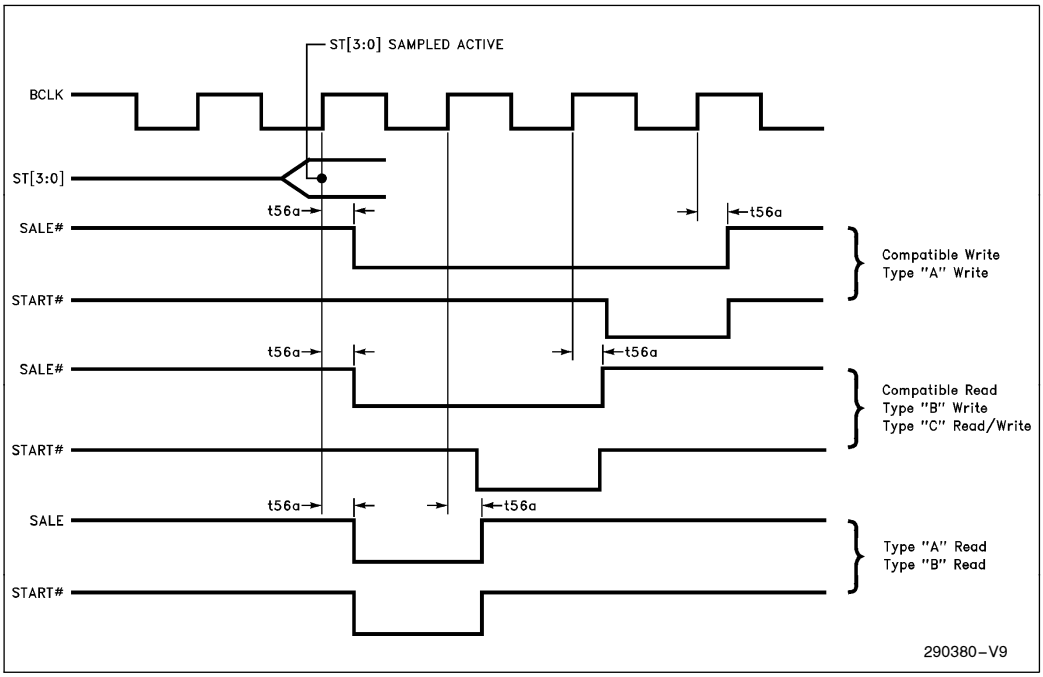


Figure 8-136. DMA Master Cycle (Single Cycle or the Initial Cycle of an Assembly or Disassembly Cycle)—t56a

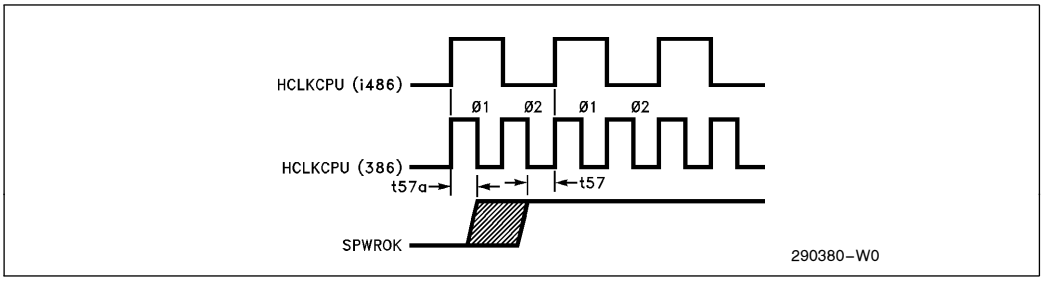


Figure 8-137. System Power-Up (SPWROK) Setup and Hold Timing—t57, t57a

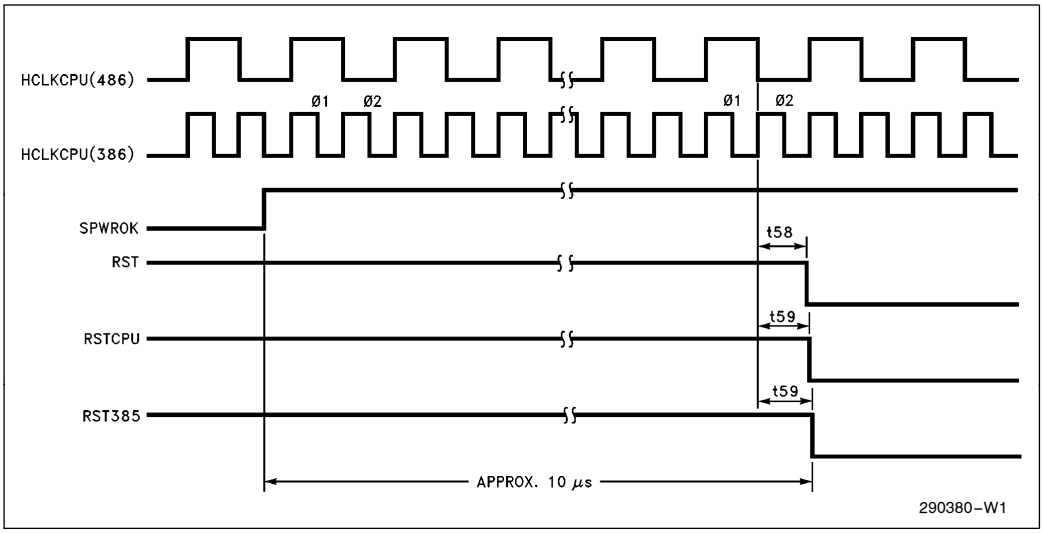


Figure 8-138. RST, RSTCPU, and RST385 During Power-Up—t58, t59

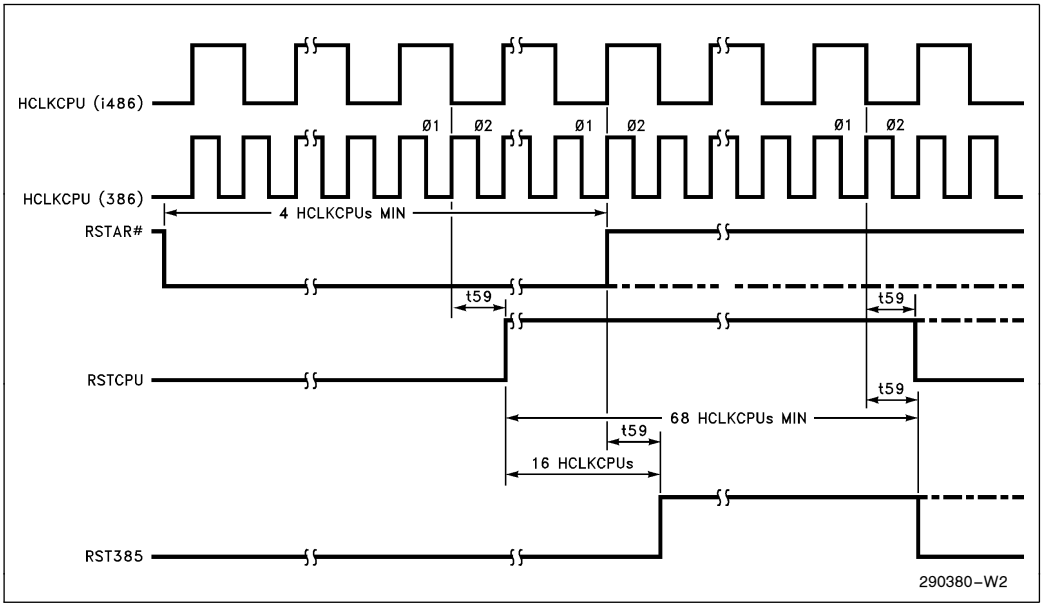


Figure 8-139. RSTCPU and RST385 During a Keyboard Reset—t59

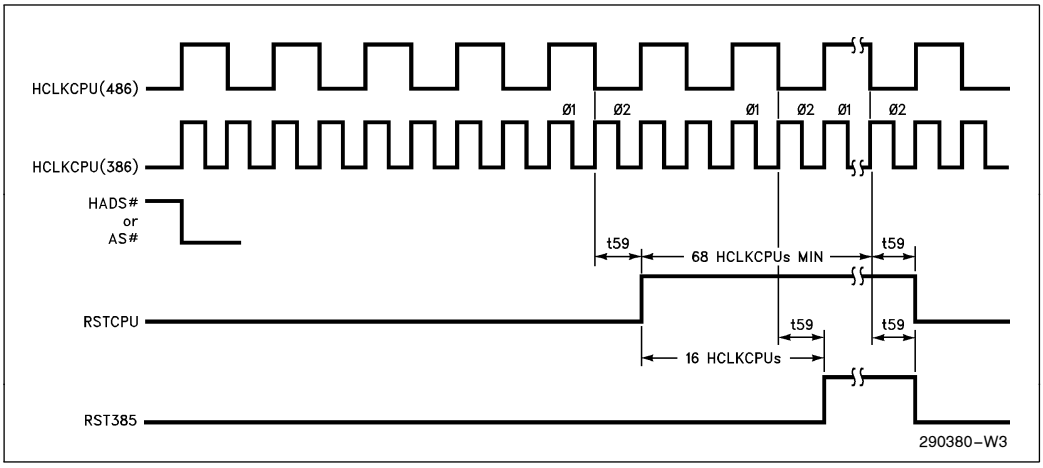


Figure 8-140. RSTCPU and RST385 During a Shutdown Cycle—t59

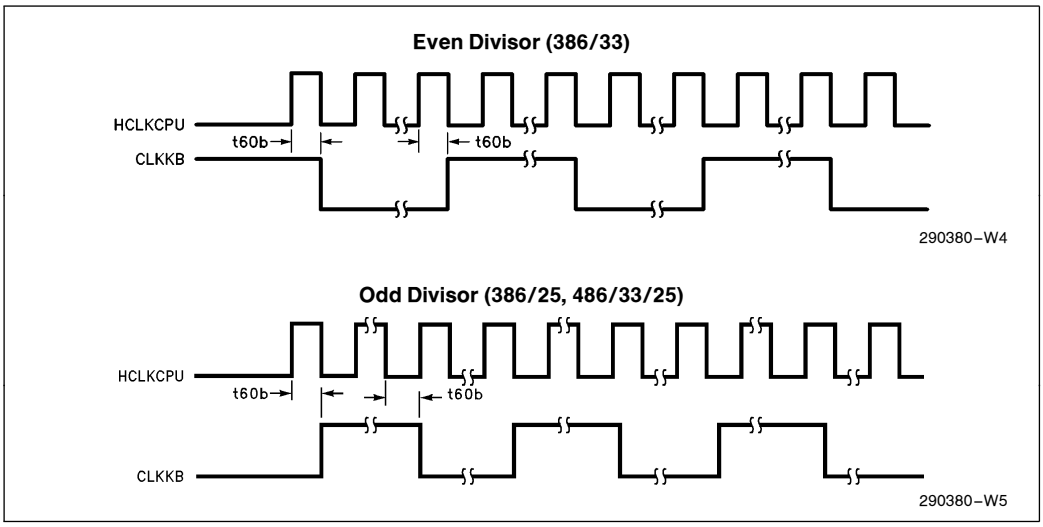


Figure 8-141. CLKKB Valid Delay—t60b

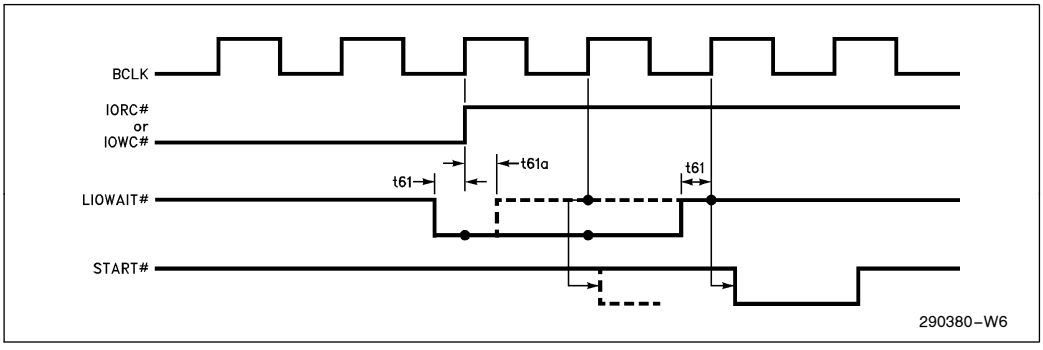
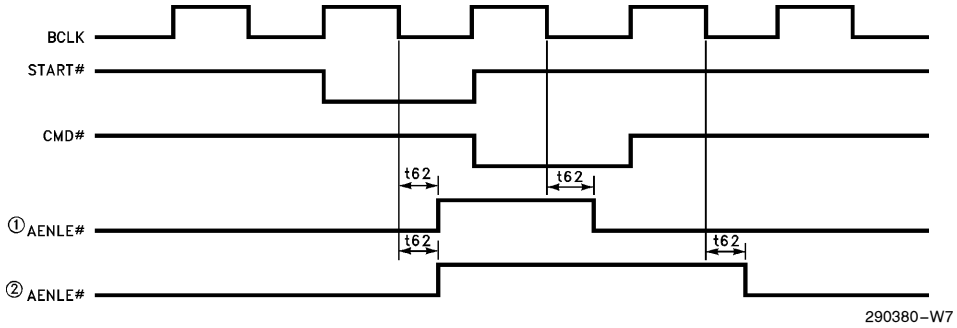
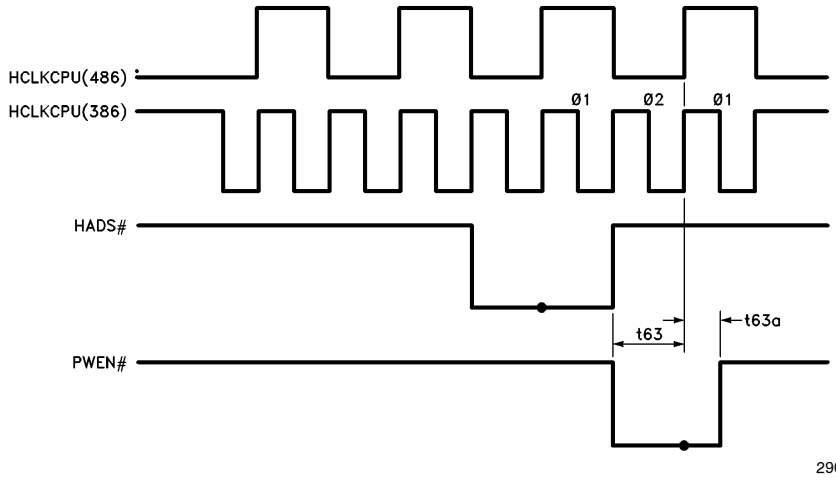


Figure 8-142. Host Master to an ISA I/O—t61, t61a



① HOST to EISA/ISA Memory or EISA I/O
② HOST to ISA I/O or ISA Memory
AENLE# rising is a valid delay from HCLKCPU rising at START# active, if BCLK is stretched (t62a).

Figure 8-143. Host Master Cycle—t62, t62a



For back-to-back cycles, PWEN# is sampled on the rising edge of HCLKCPU, at the rising edge of the CMD# signal from the first cycle. If the first cycle is an assembly or disassembly cycle, PWEN# is sampled at the end of the last CMD# of the assembly or disassembly process.

Figure 8-144. Host Master Memory Write Cycle to the EISA/ISA Bus (82350 System)—t63, t63a

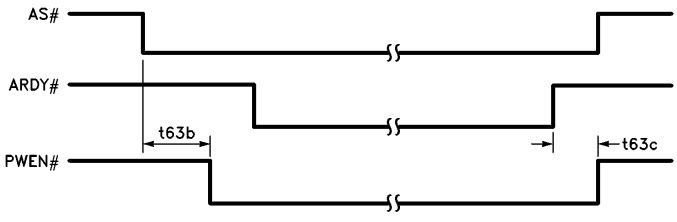


Figure 8-145. Host Master Memory Write Cycle to the EISA/ISA Bus (82350DT System)—t63b, t63c

8.4 Driver Characterization Data

As systems become more complex, and components operate at higher frequencies, further information on the performance of a component's output drivers becomes helpful or even necessary. This section offers two kinds of data relevant to the A.C. performance of the 82358DT drivers:

1. *Capacitive Derating Curves* for quickly adjusting timing delays under simplified loads.
2. *Output V/I Plots* for predicting or modeling an output's performance under more complex loads.

Here, a ''simplified load'' involves viewing the load driven by an output (traces, inputs, connectors . . .) as a sum of smaller capacitances. This method may often be valid, particularly when the trace driven is short. Longer traces, possibly with numerous stubs, present a more ''complex load'' to the output driver. Predicting an output's performance under these configurations requires a basic understanding of transmission line phenomena and possibly analog simulation tools.

The 82358DT has four different types of outputs, labeled A, B, C, and D. The following Table associates each 82358DT output with its output driver type.

82358DT Signals by Output Type

Type	Signal Name
A	BCLK
B	HNA#/SBMODE#, HRDYO#/SDVLD, SDCYPEN01#, SDCPYEN02#, SDCPYEN03#, SDCPYEN13#, SDCPYUP, SALE#
C	EX16#**, EX32#**, EXRDY**, CHRDY**, AENLE#, BALE, BE[3:0]#, CMD#, QHSSTRB#, HBE[3:0]#, HD/C#, SDHDLE[3:0]#, HDOE[1:0]#, HDSDLE1#, HERDYO#/ARDY, HHOLD, HM/IO#, HSSTRB#, HW/R#, IORC#, IOWC#, LALE#, LOCK#, MRDC#, MSBRST#, MWTC#, RST, RST385, RSTCPU, SDOE[2:0]#, SMRDC#, SMWTC#, ST0, START#, W-R, SA[1:0], SBHE#
D	IO16#**, CLKKB, HALAOE#, HALE#, LAHAOE#, LASAOE#, M-IO, SALAOE#, ST2, ST3

NOTE:
**These signals are implemented as open-drain drivers (only drives low), consequently the ''Low-to-High Transitions'' derate curve and the ''Output Driving High'' V/I plot do not apply.

To obtain capacitive derating or V/I information for a signal, first find its Type in the above Table and refer to the following sections for the appropriate curves corresponding to that Type.

8.4.1 CAPACITIVE DERATING CURVES

The following information will be useful for adjusting the given A.C. Specifications in the following two cases:

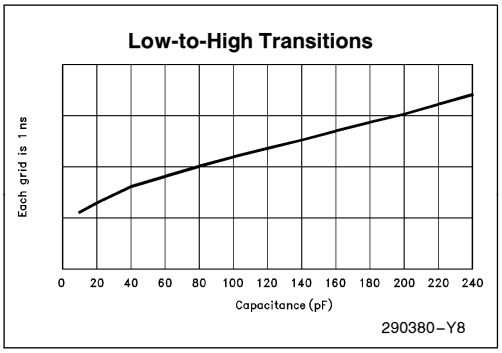
1. The actual capacitive load on a signal trace is *larger* than the specified A.C. test load. In this case, a certain amount of nanoseconds, as derived from the curves, should be *added* to the stated A.C. Specification.
2. The actual capacitive load on a signal trace is *smaller* than the specified A.C. test load. In this case, a certain amount of nanoseconds, as derived from the curves, can be *subtracted* from the stated A.C. Specification.

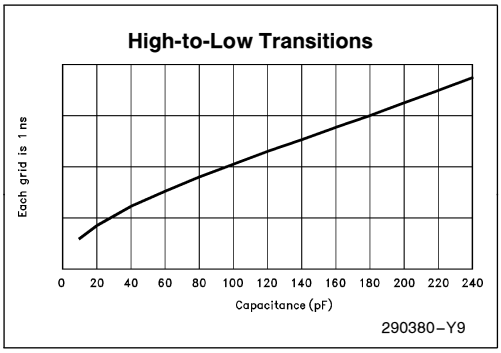
NOTE:
This information is only useful if the actual signal trace is short enough to allow viewing its loading as a lumped capacitor. If the trace is longer, and the loads more distributed, then other methods of analysis must be used to accurately assess the effects of the load.

To assist the user in applying these curves to any specification, the vertical axes show only the change in nanoseconds per gradient. Use the curves to simply determine the amount of nanaseconds to either add to, or subtract from, the given delay.

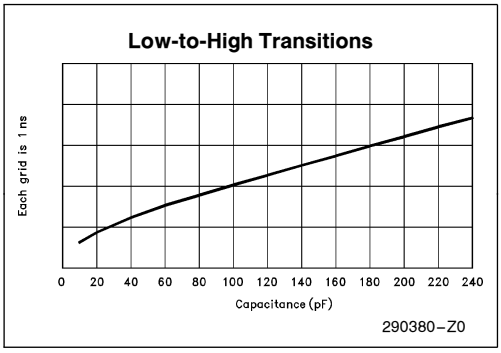
NOTE:
All derating curves are derived from design and process characteristics, and are not guaranteed by test.

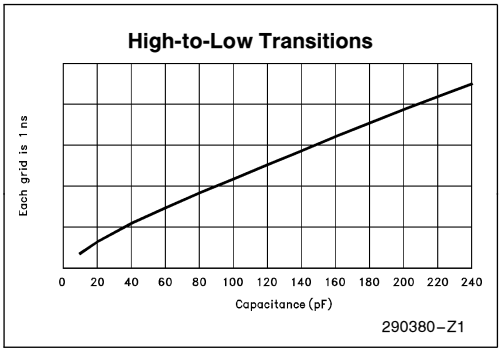
Type A Capacitive Derating Curves



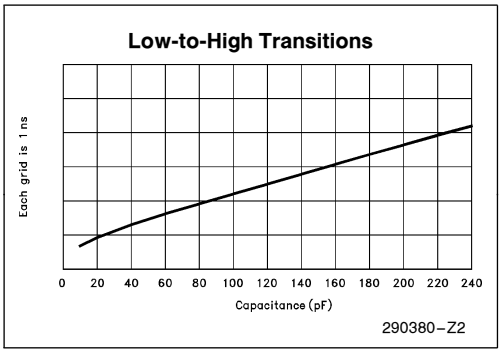


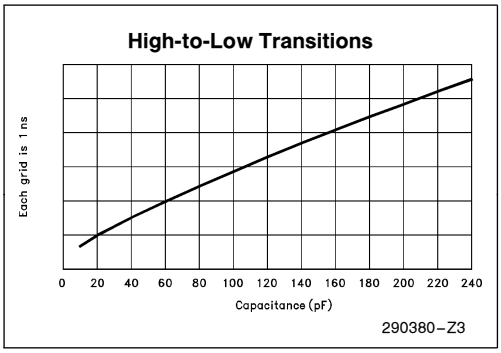
Type B Capacitive Derating Curves



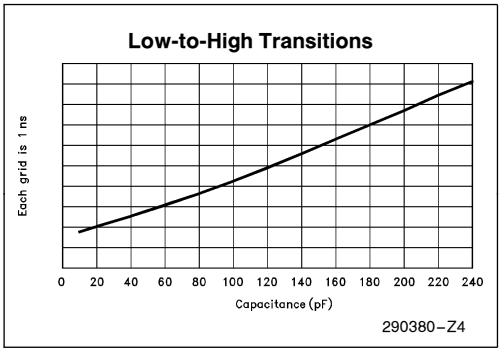


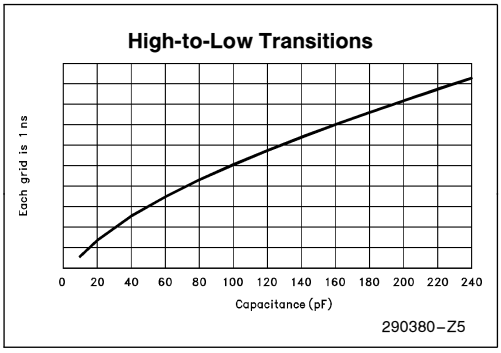
Type C Capacitive Derating Curves





Type D Capacitive Derating Curves





8.4.2 OUTPUT V/I PLOTS

Following are V/I plots for each 82358DT driver Type (A, B, C, and D). These plots can be used to obtain:

a. output modeling information

b. a measure of the instantaneous value of the output impedance

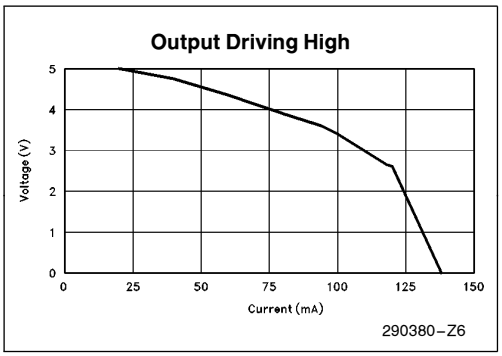
c. the magnitude of driven voltage steps through graphical analysis.

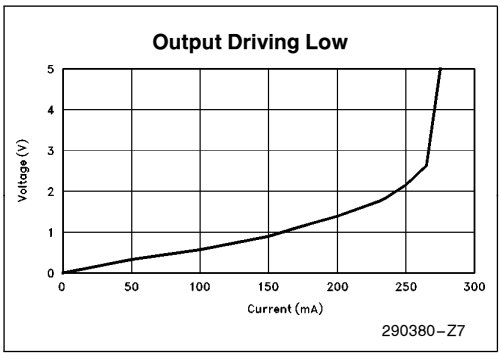
In each set of curves, a range is shown to allow best and worse case analysis over process, temperature (0°C to 85°C), and voltage 5V ± 5%).

NOTES:

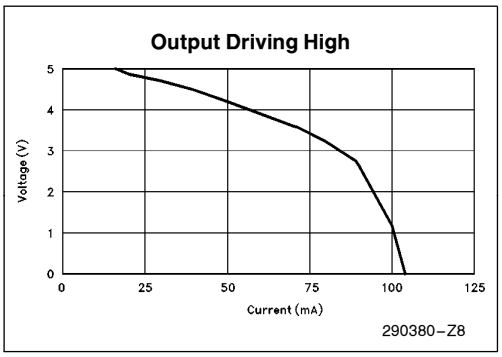
1. These plots should NOT be used to extract DC parameter data.
2. These plots are derived from process and design characteristics, and are not guaranteed by test.

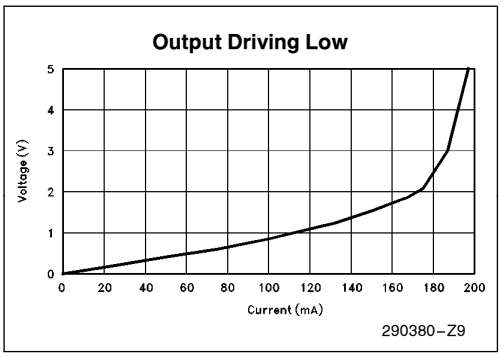
Type A V/I Plots



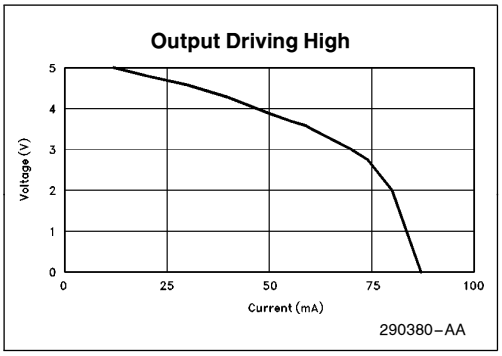


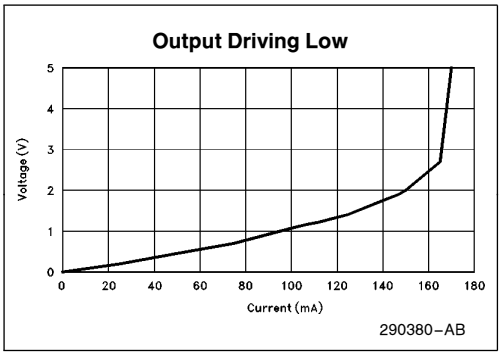
Type B V/I Plots



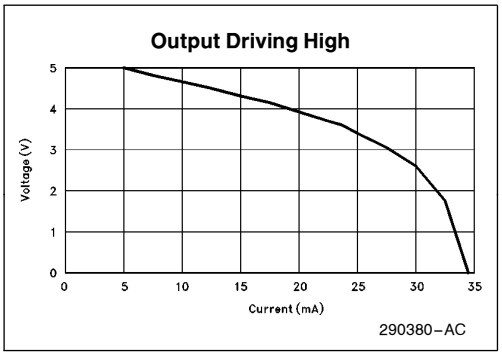


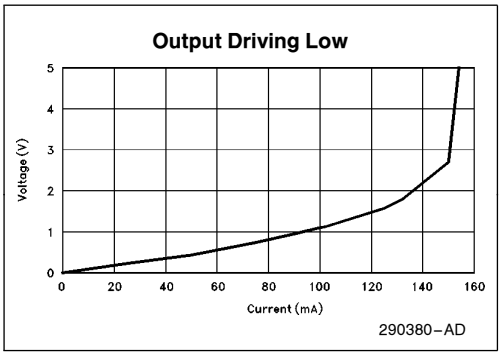
Type C V/I Plots





Type D V/I Plots





9.0 REVISION HISTORY

Revision -003 of the 82358DT data sheet contains many updates and improvements to revision -002. A revision summary of major changes is listed below:

Changes since revision -002:

Section 3.1.1 HRDYI# pin description: The HRDYI# pin description has been reworded for clarity.

Section 3.1.1 SDVLD pin description: The falling edge of SDVLD occurs after the assembly process is complete.

Section 3.1.3 HLOCMEM# and HLOCIO# pin descriptions: When used in an 82350DT system environment, AS# must be blocked from reaching the 82358DT during host or buffered master cycles not intended for the EISA or ISA bus.

Section 3.1.3 HKEN# pin description: HKEN# is used in i486™/82350 and 386/82395/82350 systems. In an 82350DT system, HKEN# should be pulled high with a 10K pullup resistor.

Section 3.2 MSBURST# pin description: A burst cycle is terminated on the rising edge of BCLK that MSBURST# is sampled inactive, unless EXRDY is sampled inactive on the previous falling edge of BCLK. In this case, CMD# will remain active until EXRDY is sampled active.

Section 3.3 CHRDY pin description: CHRDY is an output for all ISA master cycles, except cycles to ISA memory. During ISA master cycles to 8-bit EISA and ISA I/O slaves, the 82358DT will float CHRDY from the falling edge of BCLK, 4.5 ns after START# is driven inactive, if EXRDY and DRDY are sampled active.

Section 3.3 CHRDY pin description: CHRDY also takes precedence over IO16# when IO16# is used to shorten the cycle.

Section 3.3 Figure 3-2: This figure has been replaced with a new figure. The new figure provides improved clarity to the CHRDY pin description.

Section 3.4 DRDY pin description: DRDY is the indication of the end of the current transfer, until ST3 and ST2 are driven to their idle state again. After ST3 and ST2 are driven to their idle state, DRDY may still be inactive for the last transfer (burst cycles only).

Section 3.7 RST, RSTCPU, and RST385 pin descriptions: These signals are not driven active when SPWROK is driven active. They are active at powerup.

Section 3.9 BCLKIN pin description: BCLKIN should be connected to BCLK such that the delay between an HCLKCPU edge and the corresponding BCLKIN edge does not exceed 15 ns.

Section 4.12 Figure 4-28: Phase one (o1) and Phase two (o2) labeling has been added.

Section 4.14 A discussion on ‘‘Flush’’ and ‘‘Write Back’’ have been added to this section.

Section 4.15 AENLE#: For ISA slave assembly, disassembly, and i486™ burst cycles, AENLE# will remain inactive for all subsequent cycles in the assembly/disassembly or i486™ burst process.

Figure 4-34: ISA memory is grouped with ISA I/O slave cycles.

Section 4.3 Table 4-8: Note 4 has been added.

Section 5.6 DMA text section: DMA devices monitor EXRDY, and IORC# or IOWC# during read and write cycles.

Figures 5-61 and 5-63: IORC# is driven inactive if disassembly is required.

Section 5.7 Figures 5-72 and 5-73: These figures now include Write Back and Flush cycles.

Section 8.1 A.C. Specification Tables:

The following A.C. timings have been added:—t1i, t1j, t29b, t31c, t62a, and t49c.

The following A.C. timings have been improved:—t5bmin, t5bmax, t5imax, t8amax, t10cmin, t11amin, t19amax, t22cmin, t24amin, t26max, t26min, t26amin, t26bmax, t27max, t27amin, t27cmin, t30min, t33max, t34amin, t36cmin, t38amax, t45min, t45bmin, t45fmin, t45hmin, t46amin, t46cmin, t48amax, t48amin, t51max, t51min, t51amin, t51bmax, t52max, t56max, and t57min.

The following A.C. timings have been modifed:—t1gmin, t22emin, t45max, t45hmax, t47min, and t48bmax.

The following D.C. specs have been added—VIH3, Typical I_{CC} values have been added.

NOTES: Notes 16 and 17 have been added.

Section 8.3 Figure 8-15: This figure has been modified to clarify HNA# timing.

Figure 8-28: This figure has been modified to clarify HLOCMEM# and HLOCIO# timing in an 82350DT system.

Figure 8-55: The note accompanying this figure has been modified for clarity.

Figure 8-76: t29b has been added to this figure.

Figure 8-79: This figure has been modified to clarify MRDC# timing during Host or EISA master cycles to 16-bit ISA devices.

Figure 8-82: This figure has been modified to clarify SMRDC# timing during Host and EISA master cycles to 16-bit ISA devices.

Figure 8-90: This figure has been modified to clarify SA and SBHE# timing during host master BCLK stretching cases.

Figure 8-94: t39a has been removed from this figure.

Figure 8-99: This figure is for EMSTR16# not EXMASTER#.

Figures 8-102 through 8-107: The corresponding titles have been modified to clarify the figures.

Figure 8-103: At the end of the cycle, all SDCPYEN# signals are driven high from the rising edge of BCLK (t45b).

Figure 8-115: This figure illustrates EISA and DMA master cycles, not ISA master cycles.

Figure 8-124: t49c has been added to this figure.

Figure 8-129: This figure applies to an EISA master re-drive cycle, not a Host master cycle.

Figure 8-133: EISA master cases have been added to this figure.

Figures 8-139 and 8-140: These figures also apply to disassembly cycles.

Figure 8-141: This figure applies to SPWROK, not RSTAR#.

Figure 8-142: This figure was not correct. RST, RSTCPU, and RST385 are active at powerup.

Figure 8-147: This figure was not correct. AENLE#, for Host to ISA I/O or ISA memory, was inverted. Also, t62a has been added.

Section 8.4 New section (Driver Characterization Data)

82358DT Revision Summary

The following changes have been made to this document since revision 003:

Cover Page — Bullet 5 was deleted.

Section 2.1 — Paragraph 9 changed to read, ''The 82350 system supports both 386 and i486 architectures''.

Table 2.1 — Pin #127, deleted signal HBURST#. Column ''82350DT Compatible'' now reads 1 KΩ Pull-up.

Section 2.2.1 — Paragraph 2, sentence 2 was modified. The sentence now reads, ''Additonal features selectable by these mode pins are posting of memory writes to the EISA/ISA bus''.

Figure 2.4 — HBURST# was deleted.

Figure 2.6 — Updated figure and removed note.

Figure 2.7 — Updated figure and removed note.

Section 3.1.1 — Paragraph 1, sentence 3 has been changed. The sentence now reads, ''When operating in an 82350DT system environment (SBMODE# = 0), the signals function as described in the pin descriptions for signals AS#, ARDY, and SDVLD''.

The note under Host Bus Ready Input had ''EKA''. This was corrected so the sentence now reads, ''HRDYI# is not used during host master pipelined cycles to EISA or ISA slaves when ADS# for the second cycle occurs before CMD# rising of the first cycle''.

HOST BURST CYCLE INPUT (HBURST#) section was deleted.

ASYNCHRONOUS READY OUTPUT (ARDY), last sentence was deleted.

Section 3.1.2 — The note under HOST BYTE ENABLE I/O (HBE[3:0]#) has been modified. The note now reads, ''HBE[1:0]# have additional functions as described in sections 3.1.2 and 4.7''.

HOST NEXT ADDRESS/82350DT MODE I/O (HNA#/SBMODE#), last sentence in paragraph 1 was modified. The sentence now reads, ''When selected for an 82350DT environment (HNA#/SBMODE# = 0), the 82350DT host bus control signals AS#, ARDY, and SDVLD are used.

HOST BYTE ENABLES I/O (HBE0# – HBE1#), First 3 sentences in paragraph 1 were deleted.

Section 3.1.3 — The first sentence in the paragraph under HOST HOLD ACKNOWLEDGE INPUT has been modified to read, ''HHLDA is an input to the 82358DT and is synchronous to the host CPU's internal clock (HCLKCPU/2 for 386 and HCLKCPU for 486)''.

The third sentence in the paragraph under Host Bus Lock Input has been modified to read, ''HLOCK# must be sampled inactive in the EISA bus''.

Section 3.2 — The second sentence in the first paragraph under EISA Ready Input has been modified to read, ''EXRDY is an input during host master cycles to the EISA/ISA bus, EISA and ISA bus master cycles, and DMA cycles when an EISA slave responds with EX16# or EX32# asserted (refer to Table 3-4)''.

Section 3.3 — All occurrences of BCLK in the Bus Clock Output section have been changed to read ''BCLKOUT''. Table 3-3 title has been changed to read ''BCLKOUT Generation from HCLKCPU''.

Section 3.9 — The word ''immediately'' was removed from the last sentence of the Keyboard Controller Clock Output paragraph.

Sentence 2 of the Bus Clock Input was deleted and replaced with, ''References, diagrams, and specifications that use the generic term, ''BCLK'' all refer to the signal supplied to the BCLKIN input. The waveform on BCLKIN must replicate BCLKOUT (i.e., direct connect of BCLKOUT to BCLKIN, or through a non-inverting buffer)''.

Figure 4-1 — The direction of arrowheads was corrected from the LALE# to the B01__LE# and B23__LE#.

Table 4.1 — Signal HBE[1:0]# has been removed. Notes 6 for this table was removed.

Table 4.2 — Pin #127, 82350DT Compatible column, HBURST# was replaced with ''1 KΩ Pull-up''.

Section 4.1.4 — This subsection was deleted.

Figure 4-4 — This figure was deleted.

Section 5.3 — Paragraph 4 was removed.

Figure 5-3 — HADS# signal was corrected.

Figure 5-5	On signals HBE[3:0]# and BE[1:0]#, the 0110 was replaced with 1111.
Figure 5-8	HADS# signal was corrected.
Figure 5-12	This figure was deleted.
Figure 5-13	This figure is now 5-12, HBURST# signal was deleted.
Figure 5-14	This figure is now 5-13, HBURST# signal was deleted.
Figure 5-15	This figure is now 5-14, HBURST# signal was deleted.
Figure 5-16	This figure is now 5-15, HBURST# signal was deleted.
Figure 5-17	This figure is now 5-16, HBURST# signal was deleted.
Figure 5-18	This figure was deleted.
Figure 5-76	HADS# signal was corrected.
Section 6.1	HBURST# was removed.
	Signal BCLK was corrected to read BCLKOUT, and the description was corrected to read EISA/ISA Bus Clock Output.
Figure 6-1	Pin 86 name was corrected to read BCLKOUT.
Section 6.2	Pin 127, HBURST# was removed.
	Pin 86 name was corrected to read BCLKOUT.
Section 6.3	HBURST# was removed from pin 127.
Section 8.1	Symbol t5e was deleted.
	Symbol t7d was deleted.
	Symbols t12b and t12b were deleted.
	On symbol t13 parameter, the HERDYO# was removed.
	Symbol t13f was inserted.
	BCLK was corrected to read BCLKOUT.
	Symbols t31d, t31e, t31f, t31g, and t31f were added.
	Notes 18 and 19 were added.
Figure 8-2	BCLK was corrected to read BCLKOUT.
Figure 8-4	Signal BCLK was split, the diagram now reads BCLKOUT and BCLKIN. The following symbols were added in the legend:
	T_{HIGH} added t31g
	T_{LOW} added t31f
	T_{PERIOD} added t31h
Figure 8-12	This figure was deleted.
Figure 8-20	This figure was deleted.
Figure 8-31	This figure was deleted.
Figure 8-32	This figure was deleted.
Figure 8-33	On signal HERDYO#, ‘‘f’’ was added to the t13 symbols.
Figure 8-78	Signal BCLK was divided into BCLKOUT and BCLKIN, each as its own signal.
Figure 8-104	The word ‘‘a’’ has been added to the figure name. This figure name now reads, ‘‘HOST, EISA, or DMA Master Read Cycle from 16-bit ISA I/O - t45a (Active/Inactive Edges)’’.
Figure 8-142	Signal names were moved up to line up with the signal.